IEEE 3DIC 2024

- IEEE International 3D Systems Integration Conference
Sendai, JAPAN

September 25-27, 2024
Venue: September 25 Hotel Metropolitan Sendai
September 26-27 Sendai International Hotel

Advanced Program

3DIC 2024

September 25-27, 2024

Sendai, Japan

September 25 at Hotel Metropolitan Sendai

September 26-27 at Sendai Kokusai Hotel, Sendai

WELCOME FROM THE CONFERENCE CHAIRMAN

Prof. Tetsu Tanaka
Professor
Graduate School of Biomedical Engineering
Tohoku University

On behalf of the Technical Program Committee and Organizing Committee, it is our pleasure to welcome you to the IEEE International 3D Systems Integration Conference 2024 (3DIC 2024), which will be held at the Hotel Metropolitan Sendai and Sendai International Hotel in Sendai, Japan on September 25th-27th, 2024. This international conference is sponsored by the IEEE Electronics Packaging Society (EPS). The first international 3D conference was held in San Francisco in 2009 after combining the previous two 3D conferences, which were held in Tokyo in 2007 and 2008 under the sponsorship of ASET and IEEE EDS Japan and in Munich in 2003 and 2007 under the sponsorship of Fraunhofer and IEEE CPMT. The 2nd conference was held in Munich in 2010, the 3rd in Osaka in 2012, the 4th in San Francisco in 2013, the 5th in Cork in 2014, the 6th in Sendai in 2015, the 7th in San Francisco in 2016, the 8th in Sendai in 2019, the 9th in Raleigh in 2021, and the 10th in Cork in 2023, the respectively.

This year, the 11th time the conference will be held, the scope has been expanded to include 3D/Chiplets/AI semiconductors, and 46 papers will be presented as general oral presentations and poster presentations from worldwide. We are proud to announce that we have five outstanding keynote speakers and seven distinguished invited speakers from diverse backgrounds and expertise. They will discuss a wide range of key topics in the field of 3DICs and systems, providing a rich and varied experience for all attendees.
In the 3DIC 2024, 32 exhibition booths will be installed by leading companies in the electronic components, materials, packaging, and services fields to demonstrate the latest products related to 3D/Chiplets technologies. On the evening of the first conference day, September 25, a banquet will be held at the Hotel Metropolitan Sendai. Sendai is very famous for fresh seafood, delicious rice, and Sake. You can enjoy these delicious foods and sake at the banquets. The 3DIC 2024 is not just about presentations and exhibitions, but also about fostering connections and collaborations. We have designed the conference to offer you numerous opportunities for networking, in-depth discussion, and interaction with authors, speakers, and colleagues during coffee breaks, daily luncheons, and the banquet. We believe that these interactions will be as valuable as the formal sessions, and we encourage you to make the most of them to expand your professional network and learn from your peers.

We sincerely hope the 3DIC 2024 will be quite successful and you will enjoy it. We would like to thank our sponsors, exhibitors, authors, speakers, session chairs, and members of the technical program committee, organizing committee, and the local organizing committee.

3DIC 2024 CONFERENCE ORGANIZATION

3DIC 2024 ORGANIZING COMMITTEE

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Organizing Committee Co-Chair: Paul D. Franzon, North Carolina State University

Organizing Committee

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Kuan-Neng Chen, National Yang Ming Chiao Tung University
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CONFERENCE PUBLICATION CHAIR

Takafumi Fukushima, Tohoku University

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Tyndall National Institute
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In cooperation with

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3DHI 3D Heterogeneous Integration Alliance

PROGRAM-AT-A-GLANCE

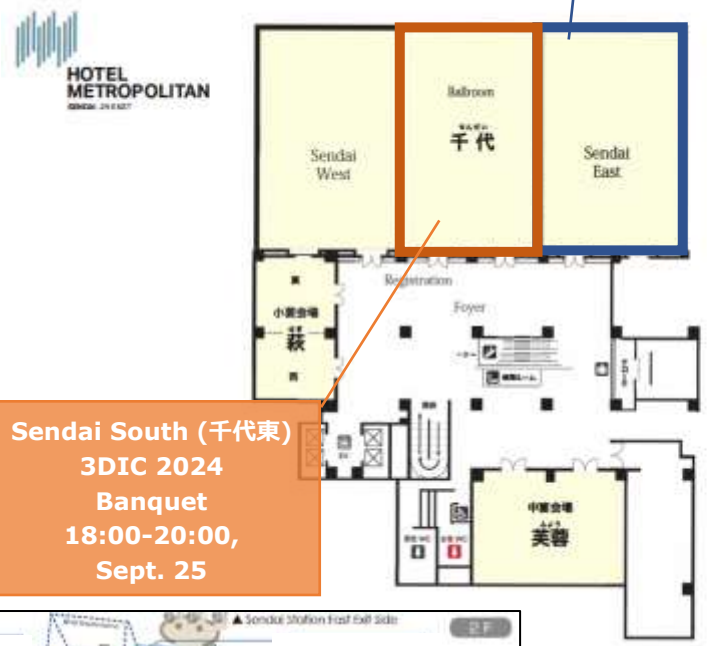
Date	25-Sep-24		26-Sep-24		27-Sep-24		
Venue	Hotel Metropolitan Sendai		Sendai Kokusai Hotel		Sendai Kokusai Hotel		NanoTerasu
Room	Sendai-East	Sendai-West/South	Heian	Heian & Foyer	Heian	Heian & Foyer	NanoTerasu Visit
9:00			Registration (8:30-)	Preparation for exhibition and poster session (8:30-10:00)	Registration (8:20-)	Preparation	
			Keynote Talk IV (8:50-9:30)		**Keynote Talk V (8:40-9:20)**		
			Invited Talk IV (9:30-10:00)		**Session 4: Design&Thermal Management (9:20-10:20)**	**Exhibition (9:00-10:35)**	
10:00			**Invited Talk V (10:00-10:30)**		Coffee Break (10:20-10:35)		
			Coffee Break (10:30-10:45)				
11:00			**Session 2: Process Technology for Hybrid Bonding (10:45-11:45)**		**Session 5 : Bumpless and Hybrid Bonding Technology (10:35-12:15)**	Dismantle by exhibitors (10:35-11:30)	
12:00	**Registration (12:00-)**		**Lunch Time (11:45-13:00)**		**Award Ceremony & Closing Remarks (12:15-12:30)**	Dismantle by organizer (11:30-12:30)	
13:00	**Opening Remark (13:00-13:10)**		**Poster Session (Core time)**	**Poster & Exhibition (10:00-18:00)**			
	Keynote Talk I (13:10-13:50)						
14:00	**Keynote Talk II (13:50-14:30)**						**NanoTerasu Visit (in Japanese) 14:00-15:00**
	Coffee Break (14:30-14:45)		**Panel Session (14:30-15:15)**				
15:00	**Keynote Talk III (14:45-15:25)**		Coffee Break (15:15-15:30)				**NanoTerasu Visit (in English) 15:00-16:00**
	Invited Talk I (15:25-15:55)		**Invited Talk VI (15:30-16:00)**				
16:00	**Invited Talk II (15:55-16:25)**		**Invited Talk VII (16:00-16:30)**				
	Invited Talk III (16:25-16:55)						
17:00	**Session 1 : Quantum Technology (16:45-17:25)**		**Session 3: Advanced Interposers (16:30-17:30)**				
18:00							
19:00		**Banquet** (18:00-20:00)					
20:00							

VENUE: HOTEL METROPOLITAN SENDAI (September 25)

1-1-1, Chuo Aoba-ku Sendai city Miyagi prefecture

* 1 minute walk from JR Sendai station west exit.

Sendai East（千代西）
3DIC 2024
Opening Ceremony
Oral Session
13:00-17:35, Sept.25
Registration starts at noon.



Sendai South (千代東)
3DIC 2024
Banquet
18:00-20:00,
Sept. 25

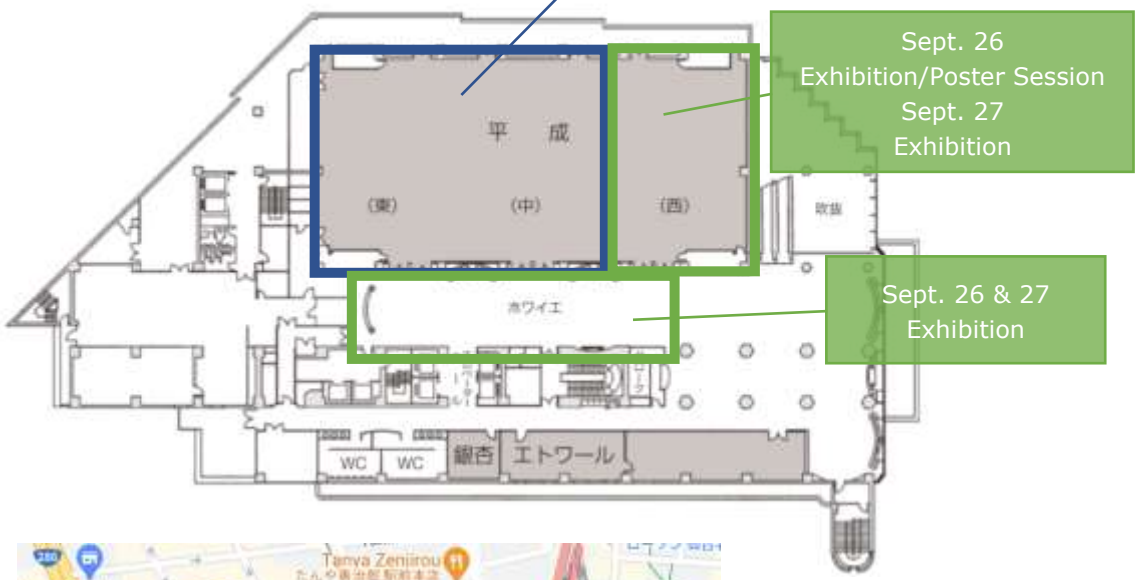
Please be noted that the 3DIC Conference Venue is **Hotel Metropolitan Sendai**, NOT Hotel Metropolitan Sendai East.
Take Sendai Station west exit to get to Hotel Metropolitan Sendai.

SENDAI KOKUSAI HOTEL (September 26-27)

4-6-1 Chuo, Aoba-ku, Sendai-shi, Sendai, Miyagi, Japan, 980-0021

* 5 minutes walk from JR Sendai station

Heisei Hall, 2F
3DIC 2024
Sept. 26 8:50-17:30 (Door open at 8:30)
Sept. 27 8:40-12:30 (Door open at 8:20)
Oral Session/Panel Session
Student Award Ceremony/
Exhibition, Poster session,
Closing Ceremony



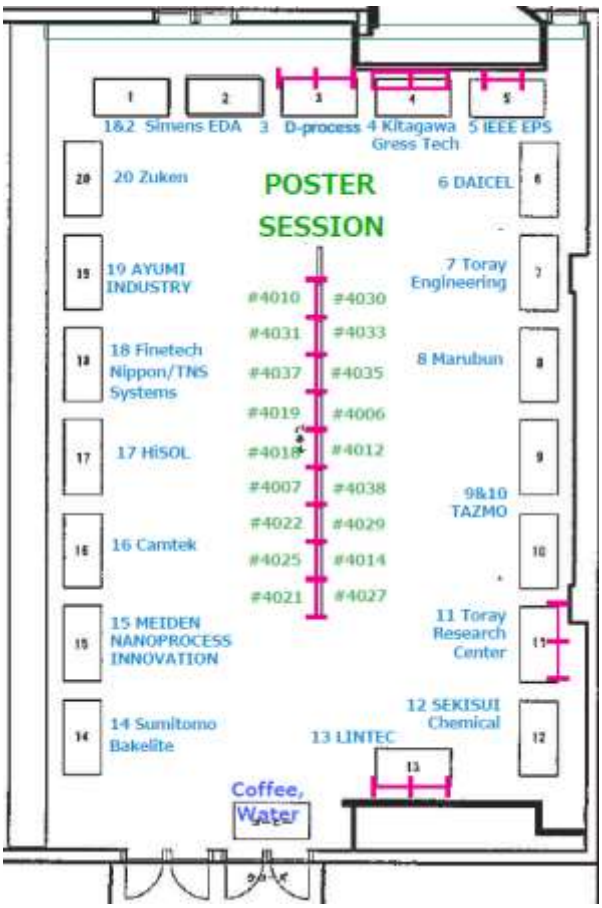
Sept. 26
Exhibition/Poster Session
Sept. 27
Exhibition

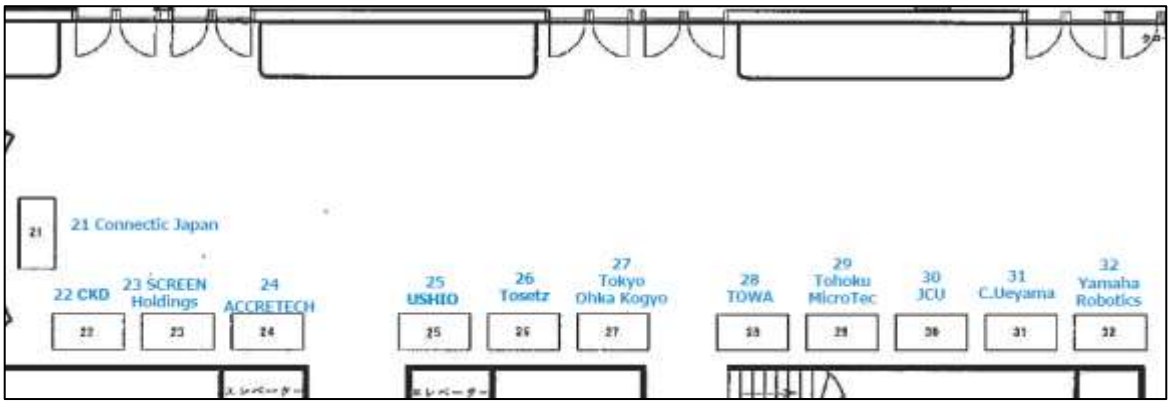
Sept. 26 & 27
Exhibition

SENDAI KOKUSAI HOTEL, Heisei Room, 2F

POSTER SESSION: September 26

EXHIBITION: September 26-27





EXHIBITORS (by alphabetical order)

Booth	Exhibitors	出展者
24	ACCRETECH	株式会社東京精密
19	AYUMI INDUSTRY CO., LTD.	アユミ工業株式会社
31	C.Uyemura &Co., Ltd.	上村工業株式会社
16	Camtek Ltd.	Camtek 株式会社
22	CKD Corporation	CKD 株式会社
21	Connectec Japan CO,Ltd.	コネクテックジャパン株式会社
6	DAICEL CORPORATION	株式会社ダイセル
3	D-process Inc.	株式会社 D-process
18	Finetech Nipon Co., Ltd.	ファインテック日本株式会社
	TNS Systems LLC	TNS システムズ合同会社
17	HiSOL, Inc.	ハイソル株式会社
5	IEEE Electronics Packaging Society	IEEE Electronics Packaging Society
30	JCU CORPORATION	株式会社 JCU
4	Kitagawa Gress Tech Co., Ltd.	北川グレステック株式会社
13	LINTEC Corporation	リンテック株式会社
8	Marubun	丸文株式会社
15	MEIDEN NANOPROCESS INNOVATIONS, INC.	明電ナノプロセス・イノベーション株式会社
23	SCREEN Holdings Co., Ltd.	株式会社 SCREEN ホールディングス
12	SEKISUI Chemical	積水化学工業株式会社
1 & 2	Siemens EDA	シーメンス EDA ジャパン株式会社
14	Sumitomo Bakelite Co., Ltd.	住友ベークライト株式会社

9 & 10	TAZMO Co., Ltd.	タツモ株式会社
29	Tohoku-MicroTec.Co.,Ltd.	東北マイクロテック株式会社
27	TOKYO OHKA KOGYO CO., LTD.	東京応化工業株式会社
7	Toray Engineering Co., Ltd.	東レエンジニアリング株式会社
11	Toray Research Center, Inc.	株式会社東レサーチセンター
26	Tosetz Inc.	株式会社 東設
28	TOWA Corporation	TOWA 株式会社
25	USHIO INC.	ウシオ電機株式会社
32	Yamaha Robotics Holdings Co., Ltd.	ヤマハロボティックスホールディングス株式会社
20	Zuken Inc.	株式会社図研

KEYNOTE TALK I

13:10-13:50, September 25

AI Computing Trends for Mobile Processor Design

Dr. Bor-Sung Liang
Senior Director, Corporate Strategy & Strategic Technology
MediaTek

Abstract:
Large-language models (LLMs) have achieved remarkable performance in many AI applications, but they require large parameter sizes in their models. The parameter sizes range from several billion to a trillion parameters, resulting in huge computation requirements for both training and inference.
Recently, there is a trend to run smaller LLMs (near or less than 10 billion parameters) on edge devices, especially for smartphones and PCs. Even though LLM model sizes are reduced, they still require more computing resources than previous mobile processor workloads and face challenges in memory size, bandwidth, and power efficiency requirements.
These trends will shape future computing architecture design and impact the semiconductor technology development. We will discuss these issues, especially mobile processor design in the generative AI era.

CV:
Dr. Bor-Sung Liang is currently a Senior Director, Corporate Strategy & Strategic Technology, MediaTek, and a Director of the Board, MediaTek Foundation. He is also concurrently serving as a Visiting Professor at Department of Computer Science and Information Engineering, EECS and GSAT in National Taiwan University, as well as a Visiting Professor at College of Electrical and Computer Engineering in National Yang Ming Chiao Tung University. He is also the Chair of IEEE CASS (Circuits and Systems Society) Taipei Chapter. He received his Ph.D degree from Institute of Electronics, National Chiao Tung University, and graduated from EMBA, College of Management, National Taiwan University.

Dr. Liang received several important awards, such as Ten Outstanding Young Persons, Taiwan; National Invention and Creation Award (one Gold Medal and two Silver Medals); Outstanding Youth Innovation Award of Industrial Technology Development Award; Outstanding ICT Elite Award; and K. T. Li Young Researcher Award.

KEYNOTE TALK II

13:50-14:30, September 25

IBM NorthPole: Brain-Inspired Neural Inference Architecture Intertwining Compute with Memory

Dr. Takanori Ueda
Staff Research Scientist
IBM Research – Tokyo

Abstract:
The rapid advancement of artificial neural networks is barely sustained by commodity computing based on the von Neumann architecture, introduced in the 1940s. While the distinct boundary between processor and memory offers significant flexibility in semiconductor manufacturing and system design, the communication between processor and memory results in performance and power overheads, known as the von Neumann bottleneck. In contrast, artificial neural networks are modeled after biological brains that have no clear boundary between compute and memory. Shouldn't processors also evolve towards a more brain-like architecture to achieve the exceptional power efficiency of the brain?
IBM NorthPole is a brain-inspired neural inference architecture that blurs the boundary by intertwining compute and memory on a chip. Once a trained AI model is fully loaded into the on-chip memory, inference results for new incoming data are calculated exclusively within the chip without accessing off-chip memory, thus overcoming the von Neumann bottleneck. The software, co-designed with the NorthPole architecture, provides an end-to-end toolchain to optimize neural networks for the architecture. The first NorthPole chip, manufactured using Global Foundries 12nm technology, compared to a GPU fabricated on a comparable 12nm process node, achieved 25 times higher energy efficiency, 5 times higher space efficiency, and 22 times lower latency.

CV:
Dr. Takanori Ueda is a researcher in the semiconductor division at IBM. His current work spans from the enablement of new semiconductor technologies to AI chip designs. He is a core member of the NorthPole project team, where he has made essential contributions, particularly in the areas of verification and physical design of the computing core. Dr. Ueda began his career in the semiconductor field in 2018, coinciding with the launch of the NorthPole project. Prior to this, his primary focus was on accelerating business workloads including microservices, database applications, and natural language processing, through his expertise in software optimization techniques.
Before joining IBM, Dr. Ueda conducted research on relational database systems. He earned his Ph.D. from Waseda University in 2013. His work has been recognized with multiple awards from academic societies.

KEYNOTE TALK III

14:45-15:25, September 25

Wafer-level 3D Heterogeneous Chiplet Integration Technology for AI and Quantum Computing Systems

Dr. Mitsumasa Koyanagi
Senior Research Fellow
Tohoku University

Abstract:
How to achieve AI chips with compact LLM and LMM models and how to scale-up quantum computing systems with high-fidelity by using the 3D integration technology will be discussed.

CV:
Mitsumasa Koyanagi received his BSc degree from the Department of Electrical Engineering, Muroran Institute of Technology Japan, in 1969 and his MSc and PhD degrees from the Department of Electronic Engineering, Tohoku University, in 1971 and 1974 respectively. He joined the Central Research Laboratory, Hitachi Co. Ltd. in 1974, where he engaged in the research of semiconductor memory (DRAM) and invented a Stacked Capacitor DRAM memory cell which has been widely used in computer
systems. In 1985, he joined Xerox Palo Alto Research Center, California, where he was responsible for the research of submicron semiconductor devices and analog/digital LSI design.

In 1988, he became a professor in the Research Center for Integrated Systems, Hiroshima University, Japan, where he engaged in the research of sub-0.1um semiconductor devices, 3-D LSI, optical interconnection. Since 1994, he has been a professor in Intelligent System Design Lab., Department of Machine Intelligent and Systems Engineering, and currently Department of Bioengineering and Robotics, Graduate School of Engineering, Tohoku University. He was awarded the IEEE Jun-Ichi Nishizawa Medal in 2006, the IEEE Cledo Brunetti Award in 1996 and the Award of the Ministry of Education, Culture, Sports, Science and Technology (Japan) in 2002, in addition to the Ohkouchi Prize in 1992, the SSDM (Solid-State Devices and Materials) Award in 1994, and the Opto-Electronic Integration Technology Award (Izuo Hayashi Award) in 2004. He is an IEEE fellow and a Japanese Applied Physics Society fellow.

KYENOTE TALK IV

08:50-09:30, September 26

CHIPS - NAPMP: Overview and Next Steps

Dr. George Orij
Deputy Director
National Advanced Packaging Manufacturing Program (NAPMP)
NIST

Abstract:
Packaging has evolved from the role of primarily protecting the chip to one of overall system integration of heterogeneous chiplets. An important aspect of this integration is miniaturization. Feature sizes such as substrate wiring pitch, die-to-substrate bonding pitch, and inter-die distances need to shrink in a predictable manner to approach monolithic wiring pitches, last level via pitches and IP block spacings. We refer to this as shrinking down of the package. Simultaneously, we need to increase the number of dies interconnected on the package to improve performance and functionality. We refer to this as scaling out of the package. Current approaches to this include additional levels in the packaging hierarchy with concomitant increases in complexity and cost. We need to think of new ways of flattening the packaging hierarchy by enabling substrates with finer wiring pitches and the ability to assemble dies at fine pitch at high throughput. Besides the technology and processes needed to accomplish this, there are other difficult issues that need to be addressed: these include power delivery and thermal dissipation, high bandwidth, and potentially active wired, wireless, and photonic connectors to the external world or between subsystems. Finally, to make this vision a reality a chiplet eco system needs to be developed with mechanical and electrical standards that ensure interoperability and a high level of reuse. Similarly, a comprehensive EDA approach needs to be developed that goes well beyond electrical abstraction of the system and includes among other things thermal, thermomechanical considerations, power delivery, test methodology and reliability. This is a challenging opportunity and promises to continue the trend set by Moore's law, for system integration.

CV:
George Orji is the Deputy Director of CHIPS NAPMP, within CHIPS R&D Office. Prior to this role, he was a Senior Program Advisor in the CHIPS R&D Office, and before then a Program Analyst in the NIST Program Coordination Office, in the Office of the NIST Director. In that role, he provided technical program and policy analysis, worked with line organizations and other staff offices on planning NIST-level strategies, program evaluation, policy coordination, budget and program initiatives, including early CHIPS Act implementation planning.
He spent more than 15 years in the NIST Labs as a project leader and mechanical engineer in the Physical Measurement, and Manufacturing Engineering Laboratories, where he led projects on nanoscale dimensional metrology, probe-based instrument and measurement methods development, uncertainty analysis, and standards development. He received his PhD in mechanical engineering from the University of North Carolina at Charlotte and is a Senior Member of both IEEE and SPIE.

KEYNOTE TALK V

08:50-09:20, September 27

TBA

Dr. Robert Patti
CEO
NHanced Semiconductors

Abstract:

CV:

Bob Patti is the owner, President, and CEO of NHanced Semiconductors, a spin-out of Tezzaron Semiconductors. Bob established NHanced to further advance and develop 2.5D/3D technologies, chiplets, die and wafer stacking, and other advanced packaging.

Prior to starting NHanced, Bob served as CTO of Tezzaron Semiconductor Corporation, a leading force in 3D integrated circuit (3DIC) technology that built its first working 3DIC in 2004. Tezzaron grew out of Bob's initial startup, ASIC Designs Inc., an R&D company specializing in high-performance systems and ASICs. During his 12 years with ASIC Designs he helped design over 100 chips.

Bob received the SEMI Award for North America in 2009, served as Vice-Chairman of JEDEC's DDRIII / Future Memories Task Group, and holds 21 US patents, numerous foreign patents, and many more pending patent applications in deep sub-micron semiconductor technologies. He holds a BSEE/CS and BSPH from Rose-Hulman Institute of Technology.

Invited Talk I

Presentation time: 15:25-15:55, September 25

Si-Substrate Backside of an IC Chip for Performance Improvements and Security

Makoto Nagata
Kobe University, Japan

Abstract:
The backside of an integrated circuit (IC) chip, more precisely, the backside surface of its Silicon substrate, provides open areas for circuit performance improvements and adversarial security attacks. These are potentially contradictory or traded off in the design of IC chip for performance and that for security. The talk overviews the benefits of engineering Si-substrate backside with additional metal routings in 2.5D and 3D advanced IC chip packaging. The talk on the contrary explains the security threats over the Si-substrate backside from both passive and active side-channel attack viewpoints. We will then discuss Si-substrate backside usage models with Si demonstration results.

Invited Talk II

Presentation time: 15:55-16:25, September 25

Paper ID: 4046

3D-Stacked 1Megapixel Time-Gated SPAD Image Sensor with 2D Interactive Gating Network for Image Alignment-Free Sensor Fusion

Ayman Abdelghafar, Kazuhiro Morimoto, Naoki Isoda, Hiroshi Sekine, Junji Iwata, Tetsuya Itano, Yasushi Matsuno, Katsuhito Sakurai, Takeshi Ichikawa
Canon Inc., Japan

Abstract: We present a 5μm-pitch, 3D-BSI 1Mpixel time-gated SPAD image sensor with 2D interactive gating network, enabling image alignment-free sensor fusion. The SPAD image sensor operates at 1,310fps for global shutter 2D imaging, and event vision sensing with 0.76ms temporal resolution under 0.02lux. Range-gated imaging result demonstrates a feasibility of robust imaging under harsh environments. The proposed gating network architecture enables robust background suppression in 3D depth measurement under 50klux ambient light.

Invited Talk III

Presentation time: 16:25-16:55, September 25

Paper ID: 4044

Superconducting Titanium Nitride in Through-Silicon Vias for 3D Integration of Qubits

Alexandra Schewski, Ulrich Schaber, Armin Klumpp
Fraunhofer EMFT, Germany

Abstract: Quantum computers based on superconducting qubits are advancing rapidly but face significant challenges in scaling to larger numbers of qubits while maintaining coherence and efficient addressing. Utilizing 3D integration with through-silicon vias (TSVs) presents a promising solution by enabling vertical signal routing and reducing interconnect crowding. This paper identifies Titanium Nitride (TiN) deposition via Metal-Organic Chemical Vapor Deposition (MOCVD) as an effective method for achieving conformal and superconductive coating of TSVs. A test structure is introduced to provide a rapid feedback loop for the development of this metallization. Additionally, a strategy is proposed to

evaluate and interpret cryogenic resistance measurements showing transitions to superconductivity. This strategy is employed to identify the influence of deposition parameters on TiN coating on TSV sidewalls and to develop a comprehensive model explaining the deposition mechanism inside TSVs.

Invited Talk IV

Presentation time: 09:30-10:00, September 26
Paper ID: 4042
Development of Hybrid Bonding: Perspectives on Material Selection, Structural Design, and Applications

Kuan-Neng Chen
National Yang Ming Chiao Tung University, Taiwan

Abstract: To achieve high-performance computing and a compact form factor in heterogeneous integration, current technology development trends in 3D ICs and advanced packaging focus on fine pitch and the size of vertical interconnections. Bonding technologies that connect two or more chips or wafers vertically are the most significant key technologies in 3D ICs. Among various bonding methods, bumpless Cu-based hybrid bonding has emerged as the primary solution to meet the demands for high speed and density. This talk will cover the platform, current status, and applications of hybrid bonding. The current development focus includes fine pitch dimensions and low-temperature hybrid bonding. A metal passivation bonding platform for extremely low-temperature bonding will be presented, along with an HRDL platform based on hybrid bonding, featuring low warpage and high layer count stacking, which can serve as an advanced RDL interposer.

Invited Talk V

Presentation time: 10:00-10:30, September 26
Paper ID: 4045
3D Flash Memory Fabricated Using CBA (CMOS Directly Bonded to Array) Technology

Shigeki Kobayashi
Kioxia, Japan

Abstract: We successfully developed CBA (CMOS Directly Bonded to Array) technology, and applied it to BiCS FLASH(TM) generation 8. Thanks to the CBA advantages, BiCS FLASH(TM) generation 8 shows superior features: an interface speed of 3.2Gbps, a program throughput of 205MB/s with 3 bits per memory cell, and a read time of 40us. Moreover, the chip size is well-scaled, using on-pitch-SGD (OPS) technology at the same time. The achieved bit density of more than 18Gb/mm2 is the world's highest in the 2xx-WL (about 218-236 WL) node. In this presentation, we review benefits of less restriction on thermal process and the increased flexibility of wiring in CBA, based on BiCS FLASH(TM) generation 8.

Invited Talk VI

Presentation time: 15:30-16:00, September 26
Paper ID: 4043
Advanced Packaging Process Technologies for Heterogeneous Integration
Noriaki Matsunaga
Applied Materials Japan, Japan
Abstract: The semiconductor industry is expected to grow over $1 Trillion, driven by AI and IoT. Advanced packaging is critical to this expansion; AI datasets and models are growing rapidly, but Moore's law is slowing down; meeting AI needs will require a move from system-on-chip to system-in-package; energy efficiency for AI computation is very important, and 3D chip stacking and heterogeneous integration are among the essential technologies enabling them. Wafer-to-wafer hybrid bonding is already being used in image sensors. And this hybrid bonding technology is further expanding its application to memory and logic devices such as Die-to-Wafer, 3D stacking and heterogeneous integration. This presentation will discuss the development of hybrid bonding technology and future challenges and solutions. Additionally, we will explore the potential of new materials and processes to further enhance performance and reliability.

Invited Talk VII

Presentation time: 16:00-16:30, September 26
Paper ID: 4047
Fan Out Panel Level Packaging Revisited
Ole Hölck
Fraunhofer IZM, Germany
Abstract: The talk will review the first wave of Fan-Out Panel Level Packaging and why it has not evolved as expected. With a look on current trends and developments, the advantages of FOPLP are considered and put in context with the likely occurence of a second wave of packaging on panel level.

PROGRAM SCHEDULE – September 25, 2024 (Hotel Metropolitan Sendai)

Opening Remark
Presentation time: 13:00-13:10, September 25
Tetsu Tanaka
Tohoku University

Keynote Talk I

Presentation time: 13:10-13:50, September 25
AI Computing Trends for Mobile Processor Design
Bor-Sung Liang
MediaTek
Abstract: Large-language models (LLMs) have achieved remarkable performance in many AI applications, but they require large parameter sizes in their models. The parameter sizes range from several billion to a trillion parameters, resulting in huge computation requirements for both training and inference.
Recently, there is a trend to run smaller LLMs (near or less than 10 billion parameters) on edge devices, especially for smartphones and PCs. Even though LLM model sizes are reduced, they still require more computing resources than previous mobile processor workloads and face challenges in memory size, bandwidth, and power efficiency requirements.
These trends will shape future computing architecture design and impact the semiconductor technology development. We will discuss these issues, especially mobile processor design in the generative AI era.

Keynote Talk II

Presentation time: 13:50-14:30, September 25
IBM NorthPole: Brain-Inspired Neural Inference Architecture Intertwining Compute with Memory
Takanori Ueda
IBM Research - Tokyo
Abstract: The rapid advancement of artificial neural networks is barely sustained by commodity computing based on the von Neumann architecture, introduced in the 1940s. While the distinct boundary between processor and memory offers significant flexibility in semiconductor manufacturing and system design, the communication between processor and memory results in performance and power overheads, known as the von Neumann bottleneck. In contrast, artificial neural networks are modeled after biological brains that have no clear boundary between compute and memory. Shouldn’t processors also evolve towards a more brain-like architecture to achieve the exceptional power efficiency of the brain?
IBM NorthPole is a brain-inspired neural inference architecture that blurs the boundary by intertwining compute and memory on a chip. Once a trained AI model is fully loaded into the on-chip memory, inference results for new incoming data are calculated exclusively within the chip without accessing off-chip memory, thus overcoming the von Neumann bottleneck. The software, co-designed with the NorthPole architecture, provides an end-

to-end toolchain to optimize neural networks for the architecture. The first NorthPole chip, manufactured using Global Foundries 12nm technology, compared to a GPU fabricated on a comparable 12nm process node, achieved 25 times higher energy efficiency, 5 times higher space efficiency, and 22 times lower latency.

14:30-14:45, September 25
Coffee Break

Keynote Talk III
Presentation time: 14:45-15:25, September 25
Wafer-level 3D Heterogeneous Chiplet Integration Technology for AI and Quantum Computing Systems」
Dr. Mitsumasa Koyanagi
Tohoku University
Abstract: How to achieve AI chips with compact LLM and LMM models and how to scale-up quantum computing systems with high-fidelity by using the 3D integration technology will be discussed.

Invited Talk I
Presentation time: 15:25-15:55, September 25
Si-Substrate Backside of an IC Chip for Performance Improvements and Security
Makoto Nagata
Kobe University, Japan
Abstract:
The backside of an integrated circuit (IC) chip, more precisely, the backside surface of its Silicon substrate, provides open areas for circuit performance improvements and adversarial security attacks. These are potentially contradictory or traded off in the design of IC chip for performance and that for security. The talk overviews the benefits of engineering Si-substrate backside with additional metal routings in 2.5D and 3D advanced IC chip packaging. The talk on the contrary explains the security threats over the Si-substrate backside from both passive and active side-channel attack viewpoints. We will then discuss Si-substrate backside usage models with Si demonstration results.

Invited Talk II
Presentation time: 15:55-16:25, September 25
Paper ID: 4046
3D-Stacked 1Megapixel Time-Gated SPAD Image Sensor with 2D Interactive Gating Network for Image Alignment-Free Sensor Fusion
Ayman Abdelghafar, Kazuhiro Morimoto, Naoki Isoda, Hiroshi Sekine, Junji Iwata, Tetsuya Itano, Yasushi Matsuno, Katsuhito Sakurai, Takeshi Ichikawa
Canon Inc., Japan
Abstract: We present a 5μm-pitch, 3D-BSI 1Mpixel time-gated SPAD image sensor with 2D interactive gating network, enabling image alignment-free sensor fusion. The SPAD image sensor operates at 1,310fps for global shutter 2D imaging, and event vision sensing with 0.76ms temporal resolution under 0.02lux. Range-gated imaging result demonstrates

a feasibility of robust imaging under harsh environments. The proposed gating network architecture enables robust background suppression in 3D depth measurement under 50klux ambient light.

Keywords: *SPAD image sensor, 3D-stacked, Backside-illuminated, Depth sensing, Time-gated*

Invited Talk III

Presentation time: 16:25-16:55, September 25

Paper ID: 4044

Superconducting Titanium Nitride in Through-Silicon Vias for 3D Integration of Qubits

Alexandra Schewski, Ulrich Schaber, Armin Klumpp
Fraunhofer EMFT, Germany

Abstract: Quantum computers based on superconducting qubits are advancing rapidly but face significant challenges in scaling to larger numbers of qubits while maintaining coherence and efficient addressing. Utilizing 3D integration with through-silicon vias (TSVs) presents a promising solution by enabling vertical signal routing and reducing interconnect crowding. This paper identifies Titanium Nitride (TiN) deposition via Metal-Organic Chemical Vapor Deposition (MOCVD) as an effective method for achieving conformal and superconductive coating of TSVs. A test structure is introduced to provide a rapid feedback loop for the development of this metallization. Additionally, a strategy is proposed to evaluate and interpret cryogenic resistance measurements showing transitions to superconductivity. This strategy is employed to identify the influence of deposition parameters on TiN coating on TSV sidewalls and to develop a comprehensive model explaining the deposition mechanism inside TSVs.

Keywords: *TSV, superconductivity, qubit, Titanium Nitride, 3D Integration*

Session 1:
Quantum Technology

Presentation time: 16:55-17:15, September 25

Paper ID: 4036

Electrochemical Deposition of Indium Thin-Films for Scalable 3D Quantum Chiplets

Jowesh Goundar, La Mai, Yugi Otake, Yuki Mori, Hideo Kosaka, Fumihiro Inoue
Yokohama National University, Japan

Abstract: This study is one of the pioneering works to explore the superconducting properties in electrochemically deposited (ECD) Indium (In) thin films. Despite extensive research on ECD Indium for its morphological and electrical properties, its superconducting characteristics remain largely unexamined. Our results reveal that a 5 μm thick ECD Indium films on Cu seed layer exhibited Type-II superconductivity which is unique from that of bulk indium . This work explores a novel material system for quantum computing applications, utilizing established ECD techniques for efficient 3D integration.

Keywords: *Electrochemical Deposition, Indium Thin-Film, Superconductivity, Quantum Chiplet, 3D Integration*

Presentation time: 17:15-17:35, September 25
Paper ID: 4008
3D Stacked Spin Qubit and TCAD Simulations
Tetsufumi Tanamoto
Teikyo Univ, Japan
Abstract: Spin qubit systems are one of the promising candidates for Si based quantum computing. The conventional spin-qubit cell consists of control and readout units around a quantum dot (QD) in which excess electron works as spin qubit. Therefore, the integration of qubits is difficult because of many wires, and extra mechanism such as shuttling parts are required. We have proposed a new structure of stacked qubits, in which the gate-all-around (GAA) channel plays the role of both the control and readout1, and the integration of qubits is feasible by extending the commercial silicon technologies. The qubit-QDs are placed in the gate insulator between the channel region and the gate electrodes like floating gates. Here, we show TCAD simulations to show how the extra electric charges in the QD affects the channel current.
Keywords: *quantum computing, spin qubits, nanosheet, surface code*

18:00-20:00, September 25
Banquet

PROGRAM SCHEDULE – September 26, 62024 (Sendai Kokusai Hotel)

Keynote Talk IV

Presentation time: 08:50-09:30, September 26

CHIPS - NAPMP: Overview and Next Steps

George Orij
National Advanced Packaging Manufacturing Program (NAPMP)

Abstract: Packaging has evolved from the role of primarily protecting the chip to one of overall system integration of heterogeneous chiplets. An important aspect of this integration is miniaturization. Feature sizes such as substrate wiring pitch, die-to-substrate bonding pitch, and inter-die distances need to shrink in a predictable manner to approach monolithic wiring pitches, last level via pitches and IP block spacings. We refer to this as shrinking down of the package. Simultaneously, we need to increase the number of dies interconnected on the package to improve performance and functionality. We refer to this as scaling out of the package. Current approaches to this include additional levels in the packaging hierarchy with concomitant increases in complexity and cost. We need to think of new ways of flattening the packaging hierarchy by enabling substrates with finer wiring pitches and the ability to assemble dies at fine pitch at high throughput. Besides the technology and processes needed to accomplish this, there are other difficult issues that need to be addressed: these include power delivery and thermal dissipation, high bandwidth, and potentially active wired, wireless, and photonic connectors to the external world or between subsystems. Finally, to make this vision a reality a chiplet eco system needs to be developed with mechanical and electrical standards that ensure interoperability and a high level of reuse. Similarly, a comprehensive EDA approach needs to be developed that goes well beyond electrical abstraction of the system and includes among other things thermal, thermomechanical considerations, power delivery, test methodology and reliability. This is a challenging opportunity and promises to continue the trend set by Moore's law, for system integration.

Invited Talk IV

Presentation time: 09:30-10:00, September 26

Paper ID: 4042

Development of Hybrid Bonding: Perspectives on Material Selection, Structural Design, and Applications

Kuan-Neng Chen
National Yang Ming Chiao Tung University, Taiwan

Abstract: To achieve high-performance computing and a compact form factor in heterogeneous integration, current technology development trends in 3D ICs and advanced packaging focus on fine pitch and the size of vertical interconnections. Bonding technologies that connect two or more chips or wafers vertically are the most significant key technologies in 3D ICs. Among various bonding methods, bumpless Cu-based hybrid bonding has emerged as the primary solution to meet the demands for high speed and density. This talk will cover the platform, current status, and applications of hybrid bonding. The current development focus includes fine pitch dimensions and low-temperature hybrid bonding. A metal passivation bonding platform for extremely low-temperature bonding will

be presented, along with an HRDL platform based on hybrid bonding, featuring low warpage and high layer count stacking, which can serve as an advanced RDL interposer.
Keywords: *Hybrid bonding, Cu-Cu Bonding, Metal Passivation, HRDL*

Invited Talk V
Presentation time: 10:00-10:30, September 26
Paper ID: 4045
3D Flash Memory Fabricated Using CBA (CMOS Directly Bonded to Array) Technology
Shigeki Kobayashi
Kioxia, Japan
Abstract: We successfully developed CBA (CMOS Directly Bonded to Array) technology, and applied it to BiCS FLASH(TM) generation 8. Thanks to the CBA advantages, BiCS FLASH(TM) generation 8 shows superior features: an interface speed of 3.2Gbps, a program throughput of 205MB/s with 3 bits per memory cell, and a read time of 40us. Moreover, the chip size is well-scaled, using on-pitch-SGD (OPS) technology at the same time. The achieved bit density of more than 18Gb/mm2 is the world's highest in the 2xx-WL (about 218-236 WL) node. In this presentation, we review benefits of less restriction on thermal process and the increased flexibility of wiring in CBA, based on BiCS FLASH(TM) generation 8.

Keywords: *3D Flash Memory, CBA, OPS*

10:30-10:45, September 26
Coffee Break

Session 2:
Process Technology for Hybrid Bonding
Presentation time: 10:45-11:05, September 26
Paper ID: 4016
A Temporary Bonding De-Bonding Tape with High Thermal Resistance, Easy Peeling and Excellent TTV for 3DIC
Moeki Nakano, Shigenori Nagahama, Toshio Takahashi, Takuya Yamamoto
SEKISUI CHEMICAL CO., LTD, Japan
Abstract: In this paper, a Temporary Bonding De-Bonding (TBDB) tape which has thermal resistance over 300 degC and easy peeling from the organic passivation on the back side wafer is introduced. Furthermore, it has so low total thickness variation (TTV) that can provide the planarization of bonding surface to perform reliable hybrid bonding. The adhesion strength of conventional TBDB tape shows >10N/inch on organic passivation such as polyimide after annealing process. To solve this problem, the method for the localization of low polarity components on the interface by thermal process is introduced. This method makes it possible to be easily peeled off from organic passivation. Newly developed TBDB tape was evaluated as feasibility conformation based upon hybrid bonding process. It has been confirmed that the back-grinding of wafer has under 3um of TTV, no delamination confirmed with thermal process up to 300 degC and it can be debonded by laser from glass

carrier, then the remaining tape is peeled off easily from wafer with polyimide passivation coat.

Keywords: *Temporary bonding de-bonding, Hybrid bonding, 3DIC, Thermal resistance, TTV*

Presentation time: 11:05-11:25, September 26
Paper ID: 4009
A Novel Direct Transfer Bonding Process with Particle Less Tapes for Die to Wafer Integration

Tomoka Kirihata{1}, Masanori Yamagishi{1}, Ichiro Sano{2}, Haruka Morita{2}, Yusuke Fumita{1}, Shinya Takyu{1}
{1}LINTEC Corporation, Japan; {2}TAZMO CO.,LTD., Japan

Abstract: Particle less tapes for Direct Transfer Bonding (DTB) have been developed that could exclude a protection layer material and coating process. Furthermore, we could get high bonding strength between dies and a wafer.

Keywords: *Particle less tape, Direct Transfer Bonding (DTB),Die to Wafer (D2W)*

Presentation time: 11:25-11:45, September 26
Paper ID: 4003
Advanced Development of Squeeze Effect Non-Contact Handling Tool for Semiconductor Chips

Hayato Hishinuma{2}, Masaaki Miyatake{1}, Hiroshi Kikuchi{2}, Yuta Tobari{2}
{1}Tokyo University of Science, Japan; {2}Yamaha Robotics Co., Ltd., Japan

Abstract: Many researchers in recent years have specifically examined direct bonding methods for semiconductor devices to improve performance and to reduce costs. As a key challenge for the direct bonding of semiconductor chips, chips must have extremely clean joint surfaces. To produce such surfaces, avoiding contact between a chip and other parts is effective. The non-contact mechanism is achieved using an ultrasonic vibration chuck. However, conventional non-contact tools cannot be installed on current bonding systems. Attachment alters measures for miniaturization and weight reduction. We made specific grooves on the vibration surface for stable levitation. By establishing a mechanism for groove (a), vibration of the chip floating area became highest. Groove (b) performed a good function with minimization of suctional variation. Additionally, we confirmed chip floating with situations of various kinds using a non-contact handling tool attached our bonder. Furthermore, we clarified the specific frequency when a non-contact tool contacted the chip unintentionally. We accomplished completely non-contact transfer using an ultrasonic squeeze effect.

Keywords: *direct bonding, non-contact tools, ultrasonic squeeze effect*

11:45-13:00, September 26
Lunch time

Poster Session Core time*
Presentation time: 13:00-14:30

Paper ID: 4010 (Poster)
Antioxidative Cu Electrodeposition for 3D Interconnects with Hybrid Bonding
Ryo Aizawa{1}, Masahiro Sawa{1}, Jinta Nampo{1}, Yurina Fukumoto{1}, Murugesan Mariappan{2}, Takafumi Fukushima{2}
{1}JCU CORPORATION, Japan; {2}Tohoku University, Japan
Abstract: We focused that the thickness of the copper oxide film varies depending on the type of acid copper plating. Generally, the oxidation reaction of Cu first produces the monovalent Cu ion Cu+, which undergoes CuOH to form a cuprous oxide Cu2O film on the Cu surface. When exposed to an oxidizing environment, cupric oxide CuO is grown. The thickness of copper oxide film formed after annealing at 150 degrees Celsius for 1 hour was measured by the sequential electrochemical reduction analysis (SERA) method, which is capable of distinguishing CuO and Cu2O. Consequently, the copper oxide film grown after annealing mainly consisted of Cu2O, and we have confirmed that the thickness of Cu2O was highly related to additive factors such as concentration and molecular weight.
Keywords: *Copper, Oxide film, Hybrid bonding, Direct bonding*

Paper ID: 4031 (Poster)
Room-Temperature and Compressive Force-Free Metal-Metal Direct Bonding for Heterogeneous Integration of Micro-Led Array on 3D-IC
Jiayi Shen, Chang Liu, Tetsu Tanaka, Takafumi Fukushima
Dept. of Mechanical Systems Engineering, Graduate School of Eng., Tohoku Univ, Japan
Abstract: In this paper, we first analyze the defects of the previous SAP process based on electroplated copper and find that the main problem of poor yield is voids in the bonding region. To address this problem, we propose an improved SAP process based on electroless plating. The isolated seed pattern of electroless plating can alleviate the void formation due to the uniform growth rate of Cu. In addition, electroless plating simplifies the processing flow and increases the reliability and yield of the SAP process.
Keywords: *Room-temperature bonding, electroless plating, micro-LED, Heterogeneous Integration*

Paper ID: 4037 (Poster)
Plasma Hydrophilic Treatment for Improved Wafer Bonding Strength via Polysilazane
Daiki Nemoto, Kai Takeuchi, Eiji Higurashi
Tohoku University, Japan
Abstract: In this paper, we present a novel wafer bonding methodology at room temperature using polysilazane as an adhesion layer. Conventional wafer bonding techniques require an annealing step, which increases the thermal budget of the process and deteriorates the reliability of the packaging structure. In this study, we combine plasma hydrophilic treatment and perhydropolysilazane (PHPS), which converts into SiO2 by reacting with water. The adsorbed water on the wafer from the plasma treatment reacts with the PHPS layer, forming the SiO2 bonding interface at room temperature. As a result, we obtained a high bond strength with a good adhesion at the wafer bonding interface.

The presented technique enables room temperature wafer bonding via a SiO2 bonding interface.
Keywords: *Wafer bonding, packaging, Si*

Paper ID: 4019 (Poster)
Cost-Effective Low-Temperature Hybrid Bonding Using Layer Transfer Technology
Yu-Lun Liu, Chun-Ta Li, Tzu-Han Sun, Chien-Kang Hsiung, Kuan-Neng Chen
National Yang Ming Chiao Tung University, Taiwan
Abstract: Hybrid bonding has become one of the most crucial technologies in the field of 3D IC. However, it requires a high degree of surface flatness and precise topography control, increasing the cost and complexity of the process. To overcome these challenges, we propose a CMP-free hybrid bonding technology by introducing layer transfer technology. In this approach, the bottom layer serves as the final hybrid bonding interface. After completing the fabrication of the hybrid bonding structure, the wafer is flipped, and laser delamination technology is used to separate the temporary carrier from the bottom layer, exposing the interface prepared for hybrid bonding. Finally, through this layer transfer process, we successfully demonstrated a CMP-free hybrid bonding process at 200°C for three minutes. The proposed cost-effective hybrid bonding technology provides a solution to the limitations of traditional solder bumps and existing hybrid bonding methods. By eliminating the need for CMP and Fly-cut processes, our approach reduces costs and increases yield, making it a promising candidate for next-generation HPC and HBM applications.
Keywords: *Hybrid bonding, Layer transfer, Temporary bonding, Laser delamination technology, High-performance computing (HPC), High-bandwidth memory (HBM)*

Paper ID: 4018 (Poster)
Characteristics of ozone-Ethylene Radical Pretreatment for Hybrid Bonding Without Water Rinsing Processes
Bungo Tanaka{2}, Tatsunori Shino{1}, Mariappan Murugesan{2}, Tetsu Tanaka{2}, Takafumi Fukushima{2}
{1}meiden nanoprocess innovations, inc., Japan; {2}tohoku university, Japan
Abstract: we demonstrate that the oer process is effective in hydrophilization for hybrid bonding without water rinsing processes. The sio2 surface is selectively hydrophilized against cu when we combine the oer pretreatment with n2 plasma activation. We will further optimize this oer process and discuss the impact on the other cu surface.
Keywords: *hybrid bonding, surface modification, hydration, hydrophilic, surface activation, ozone, hydroxyl radical*

Paper ID: 4007 (Poster)
Detectability of Resistive Open Defects with Analog Relaxation Oscillators Under Unit-to-Unit Variations of Dies
Yuya Yamahashi{3}, Yuto Ohtera{3}, Hiroyuki Yotsuyanagi{3}, Shyue-Kung Lu{1}, Masaki Hashizume{2}
{1}National Taiwan University of Science and Technology, Taiwan; {2}The Open University of Japan, Japan; {3}Tokushima Univ., Japan

Abstract: Resistive open defects may occur at Through-Silicon Vias (TSVs) or micro bumps in 3D stacked ICs during the fabrication process. In order to detect them before shipping to market, we designed a built-in test circuit based on relaxation oscillators made of only analog elements. We also developed an interconnect test method that eliminates unit-to-unit variations between dies as well as process variations of the relaxation oscillators. We examined the detectability of resistive open defects using this test method with the oscillator by Spice simulation. The results show that by embedding our built-in test circuit into dies, resistive open defects of 7.0 Ω and above occurring at interconnects between them can be detected by our test method before shipping to markets.
Keywords: *interconnect test, open defect, electrical test, 3D IC*

Paper ID: 4022 (Poster)
Gate Driver IC for GaN Power Devices Suitable for 3D Power IC
Satoshi Matsumoto{2}, Yusuke Ohgushi{1}
{1}Kyushu Institute of Technology, Japan; {2}Tokyo Metropolitan University, Japan
Abstract: 3D power IC, which GaN power devices stacked with Si based gate driver IC, is attractive. There is a problem of self-turn-on for GaN power devices. The one of the promising candidates for this problem is to provide negative power supply voltage for low side switch. However, the negative power supply voltage is usually used an external additional switching power supply and this prevents miniaturization of the power supply. Recently, capacitance of the capacitor fabricated on Si substrate(Si-Cap) is more than 1uF/mm2. Thus, the negative power supply voltage created by Si-CMOS and Si-Cap is promising for miniaturization. However, it has not been studied for gate driver IC having negative power supply voltage. In this paper, we propose gate driver IC for GaN power devices suitable for 3D IC. The negative power supply voltage is generated by negative voltage generator block. This block consists of Si-CMOS and Si-Cap. We verified the operation of 3D IC and buck converter, which is GaN power device integrated with Si-CMOS, using the proposed IC.
Keywords: *Gate driver, GaN power devices, Silicon capaciter*

Paper ID: 4025 (Poster)
3D SRAM Design & Optimization with Open Source Memory Compiler
Yuanqing Cheng{1}, Sunan Chen{1}, Chao Wu{2}, Yuan Guan{2}
{1}Beihang University, China; {2}Beijing Smartchip Microelectronics Technology Co., Ltd., China
Abstract: The rapid growth of AI and 5G increases the need for 3D SRAM, which enhances storage density and reduces data transfer, mitigating the "memory wall" issue. This paper extends an open source memory compiler OpenRAM to support automatic generation of 3D SRAM layouts, and exploring memory partitioning strategies to optimize PPA, with testcases using the 45nm 3D FreePDK library.
Keywords: *3D Integration, SRAM, Power, Performance, Area, Optimization, Design Automation*

Paper ID: 4021 (Poster)
Machine Learning-Based Diagnosis of Defects in Chiplet Interconnects

Junming Li, Huaguo Liang, Xianrui Dou, Le Yu, Zhengfeng Huang, Yingchun Lu, Cuiyun Jiang
Hefei University of Technology, China

Abstract: The diagnosis of interconnect line defects becomes increasingly difficult when integrating Chiplets in advanced packaging technologies due to the immaturity of the fabrication process, the reduction of interconnect spacing and the increase of density. In this paper, a non-destructive interconnect defect diagnosis method is proposed. Firstly, the 3D GSG TSV-RDL interconnect channels is simulated by ANSYS HFSS, and open and short defects are injected at different positions to analyze the signal integrity; using S-parameters and group delays as the features, machine learning algorithms are used to realize the classification identification and localization of defects. The results show that the algorithm used can accurately identify open and short defects; in defect localization, the mean relative error (MRE) of localization of the proposed method is less than 8%, and the Maximum Relative Error (MaxRE) does not exceed 13%. Compared with the related algorithms, the localization accuracy is significantly improved, providing a new way of interconnect testing for the identification and localization of defects inside the package interconnect line.
Keywords: *machine learning, defect diagnosis, Chiplet advanced packaging technology, interconnect channel, signal integrity*

Paper ID: 4027 (Poster)
Creep Behavior of Low-Temperature Sn-in Solder Using Nanoindentation Test
Shunya Nitta, Hiroaki Tatsumi, Hiroshi Nishikawa
Osaka University, Japan

Abstract: Nowadays, three-dimensional integrated circuits (3D ICs) require low-temperature solders to reduce heat input during soldering. Sn-52mass%In solder is promising because it has a melting point of 119 °C, which is extremely low compared to other lead-free solders. However, Sn-52mass%In solder is not widely used due to its low strength. Additionally, its low melting point may cause significant creep deformation. Therefore, this study investigates the creep behavior of Sn-52mass%In solder. Nanoindentation tests showed that the microhardness of Sn-52mass%In solder was about 40.5 MPa. The microhardness of the Sn-rich phase of Sn-58mass%Bi solder, which is a typical low-temperature solder, is about 380 MPa, and that of the Bi-rich phase is about 330 MPa. The creep test results for Sn-52mass%In solder showed a deformation index of 3.9, while the deformation index for Sn-58mass%Bi solder was 5.2, indicating that Sn-52mass%In solder is an easily creep-deformed material. These results indicated that there is room for improvement in the mechanical properties of Sn-52mass%In solder, which may be an important factor in the further evolution of 3D packaging technologies.
Keywords: *creep behavior, Low-temperature solder, nanoindentation*

Paper ID: 4014 (Poster)
16-Layer 3D Stacking Based on Self-Assembly Technology for HBM Application
Zehua Du{1}, Hiroshi Kikuchi{2}, Hishinuma Hayato{2}, Tetsu Tanaka{1}, Takafumi Fukushima{1}
{1}TOHOKU University, Japan; {2}YAMAHA ROBOTICS HOLDINGS CO., LTD., Japan

Abstract: Utilizing self-assembly technology with liquid surface tension to solve a trade-off problem between assembly time and positioning accuracy in the traditional pick-and-place method, we demonstrate 16-layer stacking with 50-μm-thick thin chips fabricated by Plasma Dicing Before Grinding (PDBG). The liquid droplets' surface tension enables the two-layer stacking of the thin dies to reach an alignment accuracy of less than 50 nm, even in a manual chip handling procedure. Examining key parameters such as initial position and liquid volume in self-assembly to address the serious trade-off issue for HBM production. We investigate the key factors to precisely align the chips and optimize the self-assembly conditions to demonstrate 16-layer stacking. The effect of liquid bridge and wetting contrast between chip surface and chip sidewall will be discussed for multi-layer fabrication.
Keywords: *self-assembly, hybrid bonding, DRAM stacking*

Paper ID: 4029 (Poster)
Temporary Adhesive Effect on Multichip Thinning for Rapid Prototyping of 3d-ic from 2d-ic Fabricated in Foundry Shuttle Services
Akihiro Tominaga, Jiayi Shen, Chang Liu, Atsushi Shinoda, Tetsu Tanaka, Takafumi Fukushima
tohoku univ., Japan
Abstract: In recent years, TSVs have also been used for CPU dies; in 3D-IC prototyping, TSV fabrication is based on wafer-level processing, so the opportunities for TSV die fabrication are very limited. To meet these requirements, we have built a technology platform to create a single 3D-IC with Cu-TSVs at the die level. This platform requires multi-chip thinning. While multi-chip thinning has been demonstrated in the past, die shift and void formation in the high temperature process required for TSV formation remained an issue to be solved. In this study, multichip thinning was demonstrated using two types of temporary adhesive materials: a blanket-type thermoplastic polymer that exhibits excellent thinning compatibility and a patterned thermosetting (B-stage) polymer that exhibits excellent fracture resistance against die shift and void formation and can be removed using chemicals and laser after TSV formation.
Keywords: *multichip thinning, tsv, temporary adhesive*

Paper ID: 4038 (Poster)
Activation of Copper Surfaces by VUV-Redox Method Using a Xenon Excimer Lamp
Shinichi Endo
Ushio Inc., Japan
Abstract: A technique for modifying the surface of a material (VUV/O3 modification) using 172 nm vacuum ultraviolet light emitted from a xenon excimer lamp is known. However, the high energy vacuum ultraviolet light and the action of active oxygen oxidize the surface of the treated material, rendering it inactive. We report the experimental results of the VUV-Redox method for surface activation of a copper sample using a vacuum ultraviolet light with an oxidizing and reducing gas.
Keywords: *VUV-Redox, Vacuum ultraviolet, 172nm, copper*

Paper ID: 4012 (Poster)
Clean Dicing: an Alternative Blade Dicing Technique for Minimising Particles in 3D Heterogeneous Integration
Akito Hiro, Damien Jon Leech, Geert Schoofs, John Slabbekoorn, Alain Phommahaxay, Koen Kennes, Gerald Beyer, Eric Beyne
imec, Belgium
Abstract: We demonstrate the suitability of a novel blade dicing technique introduced by DISCO that has an output comparable to that of plasma dicing, in terms of particle count and surface cleanliness – 'clean dicing'. This was assessed by both a simple particle counting process and image analysis of scanning acoustic microscopy data after wafer-to-wafer (W2W) bonding, showing minimal void count in the clean diced wafers.
Keywords: *Singulation, wafer to Wafer, Blade*

Paper ID: 4006 (Poster)
Impact of 2-Dimensional Materials for 3D Power IC
Satoshi Matsumoto{3}, Masataka Hasegawa{1}, Ayano Furue{2}
{1}AirMembrane Corporation, Japan; {2}Kyushu Institute of Technology, Japan; {3}Tokyo Metropolitan University, Japan
Abstract: 3D power ICs that stack Si-LSI and GaN power devices three dimensionally are promising candidates for next generation power ICs, primarily because they can minimize the power supply and realize high efficiency. However, miniaturization increases the heat generation density. One of the key problems associated with 3D power ICs is how to remove the heat. Multilayer graphene has high thermal conductivity and excellent heat removal performance. One of the most effective ways to remove heat is to directly remove it from the semiconductor chip, which is the source of heat, using multilayer graphene. In this paper, we clarify the role of multilayer graphene as a thermal interface material (TIM) and heat removal effect of multilayer graphene in 3D power ICs using thermal simulation. In addition, we propose the optimum structure using multilayer graphene, TV, h-BN, and SOI technology to realize 3D power ICs.
Keywords: *3D power IC, 2D material, Thmal interface material,*

Paper ID: 4035 (Poster)
Thermal Flow Simulation and Measurements of 3D Si Chip Stacks with TSVs
Shuhei Yokota, Rikuu Hasegawa, Kazuki Monta, Takaaki Okidono, Takuji Miki, Makoto Nagata
Kobe University, Japan
Abstract: A silicon (Si) prototype of three-dimensional (3D) digital complementary metal-oxide-silicon (CMOS) integrated circuits (ICs) was developed to simulate thermal distribution across stacked dies with through-silicon vias (TSVs) on a plastic interposer (PI) and a printed circuit board (PCB). Tested with JEDEC JESD51-2A standard temperature measurements using a thermocouple, the study showed that thermal flow from active CMOS ICs to the PCB through TSVs and PI was accurately captured in the simulation model, closely matching measurements.
Keywords: *3D-stacked-dies, Thermal flow simuation, thermocouples*

Paper ID: 4033 (Poster)
Suppression of TSV-Induced Stress by Using Negative Thermal Expansion Material
Hisashi Kino{1}, Takafumi Fukushima{2}, Tetsu Tanaka{2}
{1}Kyushu University, Japan; {2}Tohoku University, Japan
Abstract: The TSV (Through Si via) -induced stress should be considered to reduce KOZ (keep out zone). Stress relief methods such as insertion of the material with low Young's modulus have been proposed. However, it is difficult to completely relieve TSV-induced stress because materials with low Young's modulus also shrink or expand in the same direction as Cu. In this study, a novel stress relief method with negative CTE (coefficient of thermal expansion) material was proposed. Negative CTE (NCTE) materials shrink in volume as temperature increases. This characteristic means that the NCTE materials can change the volume in the opposite direction to the volume change of Cu. Therefore, NCTE materials can efficiently relieve the stress induced by Cu TSVs compared with typical materials used in TSVs.
Keywords: *negative CTE, TSV, stress*

Paper ID: 4030 (Poster)
TSV Formation Using a Direct Cu Electroplating on Electroless Plated Barrier Layer with a Low Resistivity
Yuko Ishii, Takanobu Hamamura, Tomohiro Shimizu, Takeshi Ito, Shoso Shingubara
Kansai University, Japan
Abstract: The demand for a low-cost metal filling technology to TSVs of 3D integration is increasing. In this situation, we studied a direct electroplating of Cu on an electroless plated (ELP) Co-alloy diffusion barriers formed in TSVs with a high aspect ratio. This technology enables a reduction of process steps and fabrication cost. It was shown that CoMn barrier had the lowest electrical resistivity among the Co-alloy barriers. We studied electroplated Cu filling in TSV hole by changing additive conditions on ELP barriers to obtain better Cu filling properties in TSVs. We successfully observed excellent Cu filling by the choice of the barrier metal and Cu plating bath composition for TSVs with a small diameters around 1 μ m.
Keywords: *TSV, barrier metal, electroplating,electroless plating, resistivity*

Panel Session
Presentation time: 14:30-15:15, September 26

14:30-14:45, September 26
Coffee Break

Invited Talk VI

Presentation time: 15:30-16:00, September 26
Paper ID: 4043
Advanced Packaging Process Technologies for Heterogeneous Integration
Noriaki Matsunaga
Applied Materials Japan, Japan
Abstract: The semiconductor industry is expected to grow over $1 Trillion, driven by AI and IoT. Advanced packaging is critical to this expansion; AI datasets and models are growing rapidly, but Moore's law is slowing down; meeting AI needs will require a move from system-on-chip to system-in-package; energy efficiency for AI computation is very important, and 3D chip stacking and heterogeneous integration are among the essential technologies enabling them. Wafer-to-wafer hybrid bonding is already being used in image sensors. And this hybrid bonding technology is further expanding its application to memory and logic devices such as Die-to-Wafer, 3D stacking and heterogeneous integration. This presentation will discuss the development of hybrid bonding technology and future challenges and solutions. Additionally, we will explore the potential of new materials and processes to further enhance performance and reliability.
Keywords: *Heterogeneous integration, Hybrid bonding*

Invited Talk VII

Presentation time: 16:00-16:30, September 26
Paper ID: 4047
Fan Out Panel Level Packaging Revisited
Ole Hölck
Fraunhofer IZM, Germany
Abstract: The talk will review the first wave of Fan-Out Panel Level Packaging and why it has not evolved as expected. With a look on current trends and developments, the advantages of FOPLP are considered and put in context with the likely occurence of a second wave of packaging on panel level.
Keywords: *FOPLP, FOWLP, high performance computing, chiplets*

Session 3:
Advanced Interposers
Presentation time: 16:30-16:50, September 26
Paper ID: 4011
Process Development for a Novel Low Loss and non-PFAS Photo Imageable Dielectric for RF Silicon Interposer Applications
Hamideh Jafarpoorchekab, Xiao Sun, Angel Uruena, Siddhartha Sinha, Nelson Pinho, Andy Miller, Nadine Collaert
Imec, Belgium
Abstract: Enabling 2.5/3D heterogeneous system level packaging for beyond 5G applications requires transition from PCB to other substrates such as Si. We have previously demonstrated at imec that the matter of high Si losses at higher frequencies can be resolved by inserting a metal ground plane to block Si substrate losses together with adding a thick layer of a low loss material on top such as Benzocyclobutene (BCB) to reduce transmission line losses and parasitic capacitances. However, thick BCB layers

create high warpages that are above the limit for next process steps such as photolithography and metrology. This can also lead to reliability issues such as cracks and delamination. In this work, we introduce processing of a new non-PFAS photo imageable dielectric (PID),CYCLOTENE™ XP80, with low dielectric constant (Dk) and loss tangent (Df) in high frequency ranges, up to 140GHz. This polymer has higher resolution and achievable aspect ratios than BCB. The curing condition is 200ºC/1hr vs 250ºC/1hr for BCB which in turn leads to less stress in the stack. The final warpage remains within acceptable processing limit and target CD was achieved while RF results remained in line with BCB.

Keywords: *RF Si interposer, Photo Imageable Dielectric, CYCLOTENE 遼「 XP80, Redistribution Layer, Low Loss Tangent*

Presentation time: 16:50-17:10, September 26
Paper ID: 4015
Ultra-High Density Deep Trench Capacitor (DTC) for 3DIC Integration
Hsin-Li Cheng, Jyun-Ying Lin, Ting-Chen Hsu, Chun-Yen Peng, Felix Ying-Kit Tsui, Shih-Fen Huang
Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan
Abstract: This paper introduces an ultra-high-density deep trench capacitor (DTC) for High Performance Computing (HPC) and Artificial Intelligence (AI) applications, compatible with the 3DFabric platform. The advanced DTC technology achieves a capacitance density of 2000 nF/mm² at 1.2V using cutting-edge etching and deposition techniques, and aims to further increase this to 2500 nF/mm² at 1.2V. The DTCs exhibit excellent stability, with capacitance variations under 3% over a broad temperature range and under 2% across a range of operating voltages, while maintaining ultra-low leakage currents below 20pA/nF at 1.32V. Integration with 3DFabric technologies has demonstrated significant improvements in RF impedance and voltage drop, enhancing power delivery networks in 3DICs. The development of this high-density DTC PDK marks a significant advancement in capacitor technology, offering increased miniaturization and improved performance that aligns with ongoing trends in semiconductor evolution.
Keywords: *DTC, low ESR, low ESL, 3DIC, 3DMIM, high reliabililty, CoWoS, InFO*

Presentation time: 17:10-17:30, September 26
Paper ID: 4013
Direct Sputtered Copper Seed Layer Formation on Low Dielectric Resin to Reduce Transmission Loss
Akihiro Shimizu{3}, Kazuhiro Fukada{2}, Shinichi Endo{3}, Mitsunori Abe{1}, Akiko Matsui{1}
{1}NTT Devices Cross Technologies Corporation, Japan; {2}Shibaura Machine Co., Ltd., Japan; {3}Ushio Inc., Japan
Abstract: The novelty of our direct sputtering method over conventional electroless copper plating and sputtering methods is its ability to directly form a high-adhesion copper seed layer on a smooth resin surface, eliminating the need for lower-conductivity electroless copper plating layer or adhesion layer like Ti or CuN, thereby reducing conductor loss at high frequencies and streamlining the fabrication of copper wiring patterns by omitting the catalyst removal and the adhesion layer etching process. In this study, we demonstrated

that coplanar transmission circuits fabricated using the direct sputtering method exhibit lower transmission loss at high frequencies up to 100 GHz compared to those fabricated using the electroless copper plating method, highlighting the technology's importance for next-generation communications utilizing millimeter-waves.

Keywords: *Cycloolefin polymer, Electroless copper plating seed layer, Transmission loss, Sputtering copper seed layer*

PROGRAM SCHEDULE – September 27, 2024 (Sendai Kokusai Hotel)

Keynote Talk V
Presentation time: 08:40-09:20, September27

Robert Patti
NHanced Semiconductors

Session 4:
Design&Thermal Management
Presentation time: 09:20-09:40, September 27
Paper ID: 4005
Towards 3D Ai Hardware: Fine-Grain Hardware Characterization of 3D Stacks for Heterogeneous System Integration & Ai Systems
Eren Kurshan{2}, Paul Franzon{1}
{1}North Carolina State University, United States; {2}Princeton University, United States
Abstract: 3D integration offers key advantages in improving system performance and efficiency for the End-of-Scaling era. It enables the incorporation of heterogeneous system components and disparate technologies, eliminates off-chip communication constraints, reduces on-chip latency and total power dissipation. Moreover, AIs demand for increased computational power, larger GPU cache capacity, energy efficiency and low power custom AI hardware integration all serve as drivers for 3D integration. Although 3D advantages such as enhanced interconnectivity and increased performance have been demonstrated through numerous technology sites, heterogeneous 3D system design raises numerous unanswered questions. Among the primary challenges are the temperature and lifetime reliability issues caused by the complex interaction patterns among system components. This study presents the latest drivers for 3D integration and the resulting need for hardware emulation frameworks. It then presents a design to profile power, temperature, noise, inter-layer bandwidth and lifetime reliability characterization that can emulate a wide range of stacking alternatives.
Keywords: *3D AI Hardware, AI Systems, 3D for AI, 3D Hardware Characterization*

Presentation time: 09:40-10:00, September 27
Paper ID: 4032
A Novel Multi-Chip Cooling System Using Direct On-Chip Jet Impingement for High-Performance Interposer Packages
Akshat Hetal Patel{2}, Ketan Yogi{2}, Gopinath Sahu{1}, Tiwei Wei{2}
{1}Purdue Univeristy, United States; {2}Purdue University, United States
Abstract: The current state-of-the-art cooling solution for high-performance 2.5D interposer packaging involves separately cooling logic and memory chips using different cooling methods: highly efficient solutions for high-power logic chips and less efficient ones for low-power memory chips. However, this cooling approach is not energy efficient due to excess cooling energy within the package. In contrast, our study introduces a pioneering

multi-chip cooling system utilizing direct on-chip jet impingement for these packages. A notable innovation is the integration of multiple chips within a single manifold, enabling efficient fluid transport from High Bandwidth Memories (HBMs) to Logic chips. A key design strategy is to prioritize cooling the HBMs first, leveraging their heat dissipation to preheat the working fluid and thereby reducing overall power consumption. This approach not only optimizes two-phase cooling by minimizing subcooling effects but also enhances heat transfer efficiency within the logic chips. These advancements mark a significant step forward in thermal management technology specifically tailored for demanding computing environments.
Keywords: *Multi-Chip Cooling, HPC, Interposer, HBMs*

Presentation time: 10:00-10:20, September 27
Paper ID: 4026
Thermal Analysis of Reflow Process for PIC-Embedded Package Substrate with 2.3D RDL Interposer for Co-Packaged Optics
Akihiro Noriki{2}, Hirotaka Uemura{1}, Haruhiko Kuwatsuka{2}, Naoki Matsui{1}, Reona Motoji{1}, Dan Maeda{1}, Tomoya Sugita{1}, Fumi Nakamura{2}, Takeru Amano{2}
{1}Kyocera Corporation, Japan; {2}National Institute of Advanced Industrial Science and Technology (AIST), Japan
Abstract: Toward a next generation co-packaged optics (CPO), we have worked on a novel package substrate in which photonics integrated circuits (PICs) are embedded. Compared to other works (CPO using photonics dies or sub-modules on interposer or package substrate), our proposed substrate can be provided as known good package substrate with optoelectronic conversion function and assembled in the same condition as conventional package substrates. In addition, the substrate realizes high-density optical assembly by optical redistribution layer (RDL). In this paper, we show design of the test vehicle using 2.3D electrical RDL interposer and provide its thermal analysis results for a reflow process.
Keywords: *CPO, photonics packaging, silicon photonics, 2.3D RDL interposer*

10:20-10:35, September 27
Coffee Break

Session 5:
Bumpless and Hybrid Bonding Technology
Presentation time: 10:35-10:55, September 27
Paper ID: 4002
Face-Down and Heterogeneous Chip Bonding Technology on Waffle Wafer for Bumpless Chip-on-Wafer (COW) Package
Yoshiaki Satake{1}, Tatsuya Funaki{1}, Wataru Doi{1}, Hajime Kato{2}, Shogo Okita{2}, Takayuki Ohba{3}
{1}Murata Manufacturing Co., Ltd., Japan; {2}Panasonic Connect Co., Ltd., Japan; {3}Tokyo Institute of Technology, Japan
Abstract: A high-speed manufacturable fully chiplet integration for Face-Down bonding of bumpless Chip-on-Wafer (COW) using a 300 mm waffle wafer was developed for the first time. The inkjet method successfully formed the thin adhesive layer on the waffle wafer.

There were no voids even at a 5 μm adhesive thickness and a 300 ms/chip bonding speed. More than 30,000 chips with a narrow gap of 40 μm were bonded with a misalignment of less than 10 μm. The precise bonding of different chip sizes at high speed suggests that face-down COW is promising for manufacturing-worthy heterogeneous integration.
Keywords: *Bumpless, COW, WOW*

Presentation time: 10:55-11:15, September 27
Paper ID: 4020
Low-Temperature Adhesive Hybrid Bonding Technology with Novel Area-Selective Passivation Layer
Tzu-Han Sun, Yu-Lun Liu, Chun-Ta Li, Wen-Tzu Tsai, Mu-Ping Hsu, Kuan-Neng Chen
National Yang Ming Chiao Tung University, Taiwan
Abstract: Hybrid bonding is essential for 3D IC integration, offering reduced RC delay, increased I/O density, and lower power consumption, which are crucial for heterogeneous integration. Compared with copper/oxide bonding, copper/polymer hybrid bonding offers several advantages such as cost reduction, higher bonding strength, and greater tolerance for surface roughness. This study introduces a novel low-temperature copper/polymer hybrid bonding process (150°C-200°C), using silver passivation via electroless plating, which avoids the need for additional photomasks thus reduces costs. SEM and EDX analyses confirm effective silver deposition on copper, preventing oxidation and ensuring no short-circuit issues. In the part of result, this hybrid bonding process achieves a bonding strength of 14.26 MPa and a specific contact resistance of 10-7 Ω·cm², with minimal voids observed. This method offers a low thermal budget and robust bonding, advancing 3D IC integration efficiency.
Keywords: *Electroless deposition, area selective, passivation, low temperature hybrid bonding, adhesive bonding*

Presentation time: 11:15-11:35, September 27
Paper ID: 4017
Die-to-Wafer Hybrid Bonding Impact at mm-Wave Frequencies
Mohammad Alsukour{1}, Olivier Valorge{1}, Margot Faure{1}, Loic Vincent{2}, Victor Milon{3}, Pascal Chevalier{3}, Jean-Daniel Arnould{4}, Emmanuel Pistono{4}, Christophe Dubarry{1}
{1}cea, France; {2}cime, France; {3}stmicroelectronics, France; {4}tima, France
Abstract: This paper presents the study of direct hybrid bonding metallization pads influence on a grounded coplanar waveguide (GCPW) at mm-wave up to 120 GHz. The GCPW structure is implemented in the STMicroelectronics B55X BiCMOS technology with five metal layers. The impact of the presence of hybrid bonding metallization pads, variations in their location, and the impact of the top die for die-to-wafer 3D integration. The study was conducted for a 200-μm line length. The performance, particularly in terms of attenuation loss, permittivity, and quality factor is evaluated, indicating a slight effect of hybrid bonding metallization without top die.
Keywords: *Direct Hybrid Bonding, GCPW, Radio Frequency, (Bi)CMOS technology, Compactness, mm-Wave*

Presentation time: 11:35-11:55, September 27
Paper ID: 4028
Impact of Cu Pad Density on Cu-CMP and Bonding Yield for Chip-to-Wafer Hybrid Bonding
M Mariappan{1}, H Hashimoto{1}, K Mihara{2}, T Hare{2}, T Fukushima{1}
{1}NICHe, Japan; {2}Toray, Japan
Abstract: We have proposed and demonstrated the layout design to improve the Cu-CMP quality in the TEG chip wafers for the chip-to-wafer hybrid bonding. It is inferred that the metal density around the alignment mark does impact largely the quality of Cu-CMP. The layout design with a gradual increase in the metal density between the alignment mark and the bonding Cu electrodes/pads region have resulted in the better CMP quality. We were able to minimize successfully both the dishing and the erosion of Cu electrodes, which are highly critical to realize the high-quality and high-yield chip-to-wafer hybrid bonding.
Keywords: *Metal density, Cu-CMP, Chip-to-wafer, Hybrid bonding*

Presentation time: 11:55-12:15, September 27
Paper ID: 4024
Surface Modification for Ultrasonic Cu-to-Cu Direct Bonding
Wei-Ting Chen, Chih-Hsien Chiu, Jenn-Ming Song
National Chung Hsing University, Taiwan
Abstract: Due to the advantages of low electrical resistance and size miniaturization, Cu to Cu direct bonding has become one of the important trends in microelectronic interconnect fabrication. How to achieve robust Cu-to-Cu bonding with low temperature, ambient pressure and short processing time is crucial in practical applications. To fulfill those requirements, ultrasonic technique has recently been adopted. In this study, plasma-surface modification was performed to enhance ultrasonic bonding between two electro-deposited copper bumps. Experimental results show that with a proper plasma bombardment the joint strength can be effectively raised. Remarkably, if the plasma treatment was done only on the surface of the upper bumps, the bonding performance could be further enhanced.
Keywords: *Ultrasonic bonding, plasma-surface modification, Cu/Cu direct bonding*

12:15-12:30, September 27
Award Ceremony and Closing Remark

14:00-15:00, September 27
NanoTerasu Visit in Japanese

15:00-16:00, September 27
NanoTerasu Visit in English

Tour to NanoTerasu

(advanced registration required)

Scheduled on September 27

14:00-15:00 Japanese language tour
15:00-16:00 English language tour

Facility Establisher: National Institutes for Quantum Science and Technology
Local Partners【representative office】
: Photon Science Innovation Center
Registered Institution for Facilities Use Promotion: Japan Synchrotron Radiation Research Institute
Location: NanoTerasu 468-1 Aramaki aza aoba, Aoba-Ku, Sendai-shi, Miyagi 980-0845, Japan
Site area Approx.: 60,000 sq.m
Construction cost: Approx. 38 billion yen
Electron beam energy: 3GeV
Designed stored current value: 400mA
Designed emittance: 0.9-1.1nm･rad
Linear accelerator length: 110m
Storage ring length: 349m
Beamline port: Max. 28 ports

https://nanoterasu.jp/welcome_en/

Access:
Aobayama Shuttle Bus (to/from NanoTerasu) Timetable
Aobayama Station is 9-min from Sendai Station by subway Tozai Line.
For Japanese language tour, take either 13:10 or 13:30 bus from Aobayama station. It is 9-min ride to NanoTerasu
For English language tour, take either 14:10 bus from Aobayama station.