KYENOTE TALK IV

08:50-09:30, September 26

CHIPS - NAPMP: Overview and Next Steps

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Abstract:
Packaging has evolved from the role of primarily protecting the chip to one of overall system integration of heterogeneous chiplets. An important aspect of this integration is miniaturization. Feature sizes such as substrate wiring pitch, die-to-substrate bonding pitch, and inter-die distances need to shrink in a predictable manner to approach monolithic wiring pitches, last level via pitches and IP block spacings. We refer to this as shrinking down of the package. Simultaneously, we need to increase the number of dies interconnected on the package to improve performance and functionality. We refer to this as scaling out of the package. Current approaches to this include additional levels in the packaging hierarchy with concomitant increases in complexity and cost. We need to think of new ways of flattening the packaging hierarchy by enabling substrates with finer wiring pitches and the ability to assemble dies at fine pitch at high throughput. Besides the technology and processes needed to accomplish this, there are other difficult issues that need to be addressed: these include power delivery and thermal dissipation, high bandwidth, and potentially active wired, wireless, and photonic connectors to the external world or between subsystems. Finally, to make this vision a reality a chiplet eco system needs to be developed with mechanical and electrical standards that ensure interoperability and a high level of reuse. Similarly, a comprehensive EDA approach needs to be developed that goes well beyond electrical abstraction of the system and includes among other things thermal, thermomechanical considerations, power delivery, test methodology and reliability. This is a challenging opportunity and promises to continue the trend set by Moore's law, for system integration.

CV:
George Orji is the Deputy Director of CHIPS NAPMP, within CHIPS R&D Office. Prior to this role, he was a Senior Program Advisor in the CHIPS R&D Office, and before then a Program Analyst in the NIST Program Coordination Office, in the Office of the NIST Director. In that role, he provided technical program and policy analysis, worked with line organizations and other staff offices on planning NIST-level strategies, program evaluation, policy coordination, budget and program initiatives, including early CHIPS Act implementation planning.
He spent more than 15 years in the NIST Labs as a project leader and mechanical engineer in the Physical Measurement, and Manufacturing Engineering Laboratories, where he led projects on nanoscale dimensional metrology, probe-based instrument and measurement methods development, uncertainty analysis, and standards development. He received his PhD in mechanical engineering from the University of North Carolina at Charlotte and is a Senior Member of both IEEE and SPIE.