KEYNOTE TALK III

14:45-15:25, September 25

Wafer-level 3D Heterogeneous Chiplet Integration Technology for AI and Quantum Computing Systems

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Abstract:
How to achieve AI chips with compact LLM and LMM models and how to scale-up quantum computing systems with high-fidelity by using the 3D integration technology will be discussed.

CV:
Mitsumasa Koyanagi received his BSc degree from the Department of Electrical Engineering, Muroran Institute of Technology Japan, in 1969 and his MSc and PhD degrees from the Department of Electronic Engineering, Tohoku University, in 1971 and 1974 respectively. He joined the Central Research Laboratory, Hitachi Co. Ltd. in 1974, where he engaged in the research of semiconductor memory (DRAM) and invented a Stacked Capacitor DRAM memory cell which has been widely used in computer
systems. In 1985, he joined Xerox Palo Alto Research Center, California, where he was responsible for the research of submicron semiconductor devices and analog/digital LSI design.

In 1988, he became a professor in the Research Center for Integrated Systems, Hiroshima University, Japan, where he engaged in the research of sub-0.1um semiconductor devices, 3-D LSI, optical interconnection. Since 1994, he has been a professor in Intelligent System Design Lab., Department of Machine Intelligent and Systems Engineering, and currently Department of Bioengineering and Robotics, Graduate School of Engineering, Tohoku University. He was awarded the IEEE Jun-Ichi Nishizawa Medal in 2006, the IEEE Cledo Brunetti Award in 1996 and the Award of the Ministry of Education, Culture, Sports, Science and Technology (Japan) in 2002, in addition to the Ohkouchi Prize in 1992, the SSDM (Solid-State Devices and Materials) Award in 1994, and the Opto-Electronic Integration Technology Award (Izuo Hayashi Award) in 2004. He is an IEEE fellow and a Japanese Applied Physics Society fellow.