On behalf of the Technical Program Committee and Organizing Committee, it is our pleasure to welcome you to the IEEE International 3D Systems Integration Conference 2019 (3DIC 2019) which will be held at the Hotel Metropolitan Sendai and Miyagino Ward Cultural Center in Sendai, Japan on October 8th-10th, 2019. This international conference is sponsored by the IEEE Electronics Packaging Society (EPS). The first international 3D conference was held in San Francisco in 2009 after combining the previous two 3D conferences which were held in Tokyo in 2007 and 2008 under the sponsorship of ASET and IEEE EDS Japan, and in Munich in 2003 and 2007 under the sponsorship of Fraunhofer and IEEE CPMT. The 2nd conference was held in Munich in 2010, the 3rd conference in Osaka in 2012, the fourth conference in San Francisco in 2013, the fifth conference in Cork in 2014, the sixth conference in Sendai in 2015, and the seventh in San Francisco in 2016, respectively.

The IEEE 3DIC 2019 will cover all 3D/2.5D integration topics, including process technology, materials, equipment, circuits technology, design methodology, and applications. The 3DIC 2019 Technical Program Committee has selected 65 papers which include 20 oral papers and 45 poster papers. All of these papers will provide exciting results and the latest information to attendees. Also, three outstanding keynote speakers, Prof. Subramanian S. Iyer (UCLA), Dr. Timothy M. Hancock (DARPA), and Prof. Masayuki Ohzeki (Tohoku Univ) will present quite interesting topics of 3D/heterogeneous integration and quantum computing. Furthermore, we have asked ten distinguished invited speakers to talk about various kinds of key topics. We also have a special session where the IEEE Electronics Packaging Award 2020 recipients will present the commemorative lectures. In the 3DIC 2019, 29 exhibition booths will be installed by leading companies in the electronic components, materials, packaging, and services fields to demonstrate the latest products related to 3D/2.5D technologies. On the evening of the first conference day, October 8, a banquet will be held at the Hotel Metropolitan Sendai. Sendai is very famous for fresh seafood, delicious rice, and Sake. You can enjoy these delicious foods and Sake in the banquets. The 3DIC 2019 will offer attendees numerous opportunities for networking, in-depth discussion, and interaction with authors, speakers, and colleagues during coffee breaks, daily luncheons, and the banquet.

We sincerely hope the 3DIC 2019 will be quite successful and you will enjoy it. We would like to thank our sponsors, exhibitors, authors, speakers, session chairs, and members of the technical program committee, organizing committee, and the local organizing committee.
3DIC 2019 CONFERENCE ORGANIZATION

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Paul D. Franzon – North Carolina State University

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The Murata Science Foundation
## EXHIBITORS

<table>
<thead>
<tr>
<th>Exhibitors</th>
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<tbody>
<tr>
<td>ACCRETECH</td>
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<td>Advantec Co., Ltd.</td>
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<td>KOSAKA LABORATORY LTD</td>
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<td>LINTEC Corporation</td>
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<td>Tohoku-MicroTec Co., Ltd.</td>
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<td>TOKYO OHKA KOGYO CO., LTD.</td>
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<td>12</td>
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<td>C.UYEMURA &amp; CO., LTD</td>
<td>8</td>
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### PROGRAM-AT-A-GLANCE

<table>
<thead>
<tr>
<th>Date</th>
<th>8-Oct</th>
<th>9-Oct</th>
<th>10-Oct</th>
<th>Venue</th>
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</tr>
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<tbody>
<tr>
<td></td>
<td>Hotel Metropolitan Sendai</td>
<td>Miyagino Ward Cultural Center in Sendai</td>
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<td>9:00</td>
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<td>Concert Hall</td>
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<tr>
<td>11:00</td>
<td>B3L-B Session 3: Integration Technology II (10:35-12:05)</td>
<td>C2L-B Session 6: Direct/Hybrid Bonding (10:35-12:05)</td>
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<tr>
<td>12:00</td>
<td>Lunch (12:05-13:30)</td>
<td>Lunch / TPC meeting (12:05-13:30)</td>
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<td>13:00</td>
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<td>14:00</td>
<td>A1L-A Plenary Talk I (13:30-14:10)</td>
<td>B4P-C Poster Session (Core time: 13:30-15:00)</td>
<td>C3L-B Session 7: Thermal Management (13:30-15:00)</td>
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<tr>
<td>15:00</td>
<td>(continued) A2L-A Session 1: 3D Stacked Imager (14:10-16:05)</td>
<td>B5L-B Session 4: Memory System (15:00-16:40)</td>
<td>Break (15:00-15:15)</td>
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<tr>
<td>16:00</td>
<td>Break (16:05-16:20)</td>
<td>B6L-B Session 5: Monolithic/Hetero Integration (16:55-18:05)</td>
<td>C4L-B Session 8: Student Award Ceremony &amp; Closing</td>
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</tr>
<tr>
<td>18:00</td>
<td>Break (18:05-18:20)</td>
<td>B7L-B Panel Session (18:20-19:20)</td>
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VENUE: HOTEL METROPOLITAN SENDAI (1st Day, Oct. 8)

Please be noted that the 3DIC Conference Venue is Hotel Metropolitan Sendai, NOT Hotel Metropolitan Sendai East. Take Sendai Station west exit to get to Hotel Metropolitan Sendai.
VENUE: MIYAGINO WARD CULTURAL CENTER (Oct. 9-10)

- **Concert Hall (PaToNa Hall)**
  - 3DIC 2019
  - Oral Session/Panel Session
  - Student Award Ceremony/
    Closing Ceremony
  - October 9-10
  - The door open is 8:45 at earliest.

- **Theater Hall (PaToNa Theather)**
  - Poster Session
  - Exhibition
  - Coffee Break
  - October 9-10

- **#1 Meeting Room (2F)**
  - Lunch Room
  - October 9-10
  - Bring your lunch

- **#3 Meeting Room (3F)**
  - Lunch Room
  - October 9-10
  - Bring your lunch
POSTER SESSION/EXHIBITION AT MIYAGINO WARD CULTURAL CENTER (October 9-10)  1F Theater Hall (PaToNa Theater)

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15. BN Technology  
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17. LINTEC Corporation  
18. Hitachi Chemical Co., Ltd.  
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PLENARY TALK

13:30-14:10, October 8, 2019 Paper ID: 4073

On why dielets are the new craze for heterogeneous Integration

Prof. Subramanian S. Iyer
Distinguished Professor, Electrical Engineering Department,
Material Science and Engineering Department,
Henry Samueli School of Engineering and Applied Science, UCLA, USA

<Abstract>
Chiplets (or more accurately dielets) are the new thing in heterogeneous systems integration. In this talk, we will review why this makes sense and what the criteria for dielet selection are. Dielet selection depends on functionality and reuse potential but are constrained by yield, handling and testing. This limits the die size to between 1 and 100 mm². The technologies that will be used to implement this concept are diverse and application dependent. They will require new substrate and assembly technologies. The dielet approach has significant challenges in both the infrastructure as well as the ecosystem. These include a secure supply chain and diversity of dielets. We will discuss those as well. We will introduce two heterogeneous integration platforms the SiIF and Flextrate to demonstrate these ideas. The dielet concept is gaining momentum and offers a good way to leverage the solid existing semiconductor infrastructure and make advanced packaging a much more value-add component of the technology.

<CV>
Subramanian S. Iyer (Subu) is Distinguished Professor and holds the Charles P. Reames Endowed Chair in the Electrical Engineering Department and a joint appointment in the Materials Science and Engineering Department at the University of California at Los Angeles. He is Director of the Center for Heterogeneous Integration and Performance Scaling (CHIPS). Prior to that he was an IBM Fellow. His key technical contributions have been the development of the world’s first SiGe base HBT, Salicide, electrical fuses, embedded DRAM and 45nm technology node used to make the first generation of truly low power portable devices as well as the first commercial interposer and 3D integrated products. He also was among the first to commercialize bonded SOI for CMOS applications through a start-up called SiBond LLC. More recently, he has been exploring new packaging paradigms and architectures that they may enable including in-memory analog compute. He has published over 300 papers and holds over 70 patents. He was a Master Inventor at IBM. He has received several outstanding technical achievements and corporate awards at IBM. He is an IEEE Fellow, an APS Fellow and a Distinguished Lecturer of the IEEE EDS and EPS as well as the treasurer of EDS and a member of the Board of Governors of IEEE EPS. He is also a Fellow of the National Academy of Inventors. He is a Distinguished Alumnus of IIT Bombay and received the IEEE Daniel Noble Medal for emerging technologies in 2012.

List of publications/patents:
https://scholar.google.com/citations?user=xXV4oIMAAAAJ&hl=en
PLENARY TALK

09:00-09:40, October 9, 2019 Paper ID: 4074

Heterogeneous and 3D Integration at DARPA
Dr. Timothy M. Hancock
Program Manager, Microsystems Technology Office
Defense Advanced Research Projects Agency (DARPA), USA

<Abstract>
Next generation electronic systems face the challenges of signal interconnect in an increasing dense fashion will use diverse technology sets that requires an unprecedented level of complexity at the board, package and chip level. This paper will focus on the problems facing the commercial and defense community and how DARPA investments in heterogeneous and 3D integration are tackling this challenge. Work from the Diverse Accessible Heterogeneous Integration (DAHI) program will be the primary focus and will highlight the use of dielet bonding and wafer-scale bonding of CMOS with InP, GaN and GaAs for use in wideband RF and mixed-signal systems. Some of the challenges and successes of integrating a diverse set of compound semiconductors will be presented. Beyond DAHI, an overview of the Common Heterogeneous Integration and IP Reuse Strategies (CHIPS) program will be presented where the focus is on the reuse of CMOS dielet building blocks as an alternative to low-volume ASIC development. Finally, early work in the 3DSOC program will highlight how 3D monolithic integration may help break the memory wall at relaxed lithography nodes. Potential future directions for continued research will be discussed.

<CV>
Dr. Timothy M. Hancock joined DARPA as a program manager in September 2016 where his research interests revolve around RF microsystem development that spans semiconductor device processing, circuit design and system integration for communication, radar and electromagnetic spectrum sensing applications. Dr. Hancock is serving DARPA while on leave from MIT Lincoln Laboratory where he was an assistant group leader in the RF Technology Group and led programs in RF system design, RF & mixed signal integrated circuit design in CMOS and SiGe as well as material & device development for next generation RF GaN-on-Si and emerging ultra-wide bandgap semiconductors. In his first seven years at the Lincoln Laboratory as a staff member, he worked he developed low-power wireless devices for multiple applications and several multiple-input, multiple-output (MIMO) communication systems.
Dr. Hancock has published more than 25 papers and is a senior member of the IEEE, where he has served on the technical program committee for the Radio Frequency Integrated Circuits (RFIC) Symposium and the steering committee of the International Microwave Symposium. In 2010 he was inaugural recipient of the MIT Lincoln Laboratory Early Career Technical Achievement Award. Dr. Hancock earned the BS degree in electrical engineering from the Rose-Hulman Institute of Technology and the MS and PhD degrees in electrical engineering from the University of Michigan.
PLENARY TALK

09:40-10:20, October 9, 2019 Paper ID: 4075

Quantum annealing and its application - new generation of natural computing
Prof. Masayuki Ohzeki
Associate Professor, Graduate School of Information Sciences
Tohoku University, Japan

<Abstract>
Quantum annealing is a generic solver for optimization problems, which uses fictitious quantum fluctuation. The most groundbreaking progress in the research field of quantum annealing is its hardware implementation, that is, the so-called quantum annealer, by using artificial spins. In this presentation, we demonstrate several applications of quantum annealing in real industry after a short introduction.

<CV>
Masayuki Ohzeki graduated with a Ph.D. in physics from Tokyo Institute of Technology in 2008, and subsequently spent one and a half years as a postdoctoral fellow. He worked as an assistant professor in the Kyoto University. Since 2016, he has been an associate professor at the Graduate School of Information Sciences at Tohoku University. His research interests are broad, including machine learning and its potential from a perspective of theoretical physics and itself. He was awarded the 6th Young Scientists' Award of the Physical Society of Japan, and the Young Scientists' Prize by The Commendation for Science and Technology by the Minister of Education, Culture, Sports, Science and Technology in 2016.
<Abstract>
Nowadays, the Internet-Of-Things (IoT) consists of a variety of LSIs. To use in different situations, small, multi-functional and high-performance LSIs have been strongly needed. One promising solution is System-In-Package (SiP) such as multi chip 2D package and 3D stack package. 3D chip stacking technology in particular can easily implement different function chips in a small system. We have contributed to the development of multifunctional, high-performance products with various 3D chip stacking technologies for many years. We have developed a CIS device with metal wiring under the photo-diode, which is called a back-illuminated CIS (BI-CIS). We confirmed that the device offers higher sensitivity and better performance in optical shading without any degradation in the device performance. This BI-CIS is ideally suited to applications requiring high picture quality from a small pixel size. The wafer-to-wafer bonding technology was newly introduced for the fabrication of BI-CIS. The size of CIS chips, especially for the mobile devices, were so small that the high manufacturing yield could be achieved with wafer-to-wafer bonding method. In addition to the imaging quality that conventional image sensors require, there was high demand for new functions that can respond to various photo-taking scenes. We have developed a stacked BI-CIS, composed of conventional BI-CIS technology and standard logic technology. The stacked BI-CIS layers back-illuminated structure pixels onto chips containing the circuit section for signal processing in place of carrier wafer in conventional BI-CIS. The newly attached logic circuits have achieved the advanced features such as higher sensitivity and high dynamic range (HDR) movie. In the early types of stacked BI-CIS the through-silicon-via (TSV) technology was used to electrically connect CIS chip and logic circuits. To improve the manufacturing productivity, we have recently introduced the wafer-level Cu-Cu hybrid bonding technology in place of TSV technology. The Cu-Cu hybrid bonding technology provides us further merits such as fine-pitch and large-scale connection and hence additional new functions."

<CV>
Yoshihisa Kagawa is a senior manager of Research Division, Sony Semiconductor Solutions Corporation. He received his B.S. and M.S. degrees from Kyoto University, Japan in 1999 and 2001, respectively. He joined Sony Corporation in 2004, where he has been a specialist for BEOL process integration. Currently, he manages the process integration for the CMOS image sensor. He is especially focused on developing the Cu-Cu hybrid bonding technology for stacked CMOS image sensor.
<Abstract>

With the advent of the IoT era, more and more sensors are expected to be used in the future. The sensor needs an ADC that converts signals to digital values, but the sensor has different specifications such as signal bandwidth and dynamic range depending on the application. So far, ADCs of various conversion methods and performance have been developed according to the required specifications, but development efficiency is low, and development will be difficult if this is left as it is. Therefore, in this talk, we will discuss the possibility of ADC that can address many applications and required specifications with one ADC, while incorporating the latest technology trends.

<CV>

Akira Matsuzawa received B.S., M.S., and Ph. D. degrees in electronics engineering from Tohoku University, Sendai, Japan, in 1976, 1978, and 1997 respectively. In 1978, he joined Matsushita Electric Industrial Co., Ltd (Panasonic). Since then, he has been working on research and development of analog and Mixed Signal LSI technologies. On April 2003, he joined Tokyo Institute of Technology and has been a professor on physical electronics. He retired from Tokyo Institute of Technology on March 2018 and becomes an honorary professor. Now he is a president of Tech Idea Co., Ltd., founded by himself. He received the IR100 award in 1983, the R&D100 award and the remarkable invention award in 1994, the ISSCC evening panel award in 2003, 2005, 2015, MEXT science and technology award in 2017 and IEICE Achievement Award in 2019. He is an IEEE Fellow since 2002, and an IEICE Fellow since 2010.
INVITED TALK

16:20-16:50, October 8, 2019 Paper ID: 4080

Power-Performance Advantages of InFO Technology for Advanced System Integration

Dr. Chuei-Tang Wang
Technical Director, R & D
Taiwan Semiconductor Manufacturing Company Limited (TSMC), Taiwan

<Abstract>
Since 2012, the development of InFO technology has gained much attention in semiconductor industry as it leads a new wafer level system integration (WLSI) development direction. The technology leverages foundry wafer process experience and Cu back end of line (BEOL) capability to provide thin dielectric layer, fine pitch RDL and vertical interconnect for system designers the flexibility to design 3D system, multiple chip system and RF/Analog system, respectively. The InFO has a unique position in the TSMC WLSI platform from package size and IO counts for mobile, IoT and HPC applications. In the paper, the power integrity, signal integrity and RF performance of the technology in the applications will be reported. For power integrity, excellent performance from thin dielectric layers and integration of low equivalent series inductance (ESL) integrated passive devices (IPD) is studied. The technology has 38% lower power delivery networking (PDN) impedance and 17% lower voltage droop, compared to flip chip substrate. For bandwidth performance, the effect of line width on data rate and line density is studied. At the finest line width, the InFO can provide more than 1,000/mm interconnect lines between chips. The bandwidth density for the finest line (1x) is about 2.5 times higher than that for the coarse line (2.5 x). The bandwidth densities of various technologies, such as MCM, Fan Out, Si Bridge, Si Wafer and InFO are compared. A record high 10 Tbps/mm of bandwidth density is obtained by submicron RDL In FO. Finally, a 3D solenoid InFO inductor is demonstrated. The inductor, formed by Cu via and RDL achieve s 0.68x lower resistance and 1.6x higher Q factor, compared to 2D spiral inductor at the same inductance. From the above study, we can conclude the InFO technology provides superior power performance advantages from thin dielectric and flexible RDL pitch for mobile to HPC product applications.

<CV>
Chuei-Tang Wang received the B.S. and M.S. degrees in materials science and engineering from National Tsing Hua University, Hsinchu, Taiwan, in 1983 and 1985, respectively, and the Ph.D. degree from Stanford University, Stanford, CA, USA, in 1997. He joined USI in Nantou, Taiwan and led wireless connectivity SiP module design in 1999. Later he was responsible for system miniaturization technology development. In 2011, he joined TSMC Integrated Interconnect and Packaging (IIP) RD team as a Technical Director for system architecture and SI, PI and RF performance study. He had received a National Award of Industrial Technology Advancement (ITA), Taiwan, for the leadership of connectivity SiP module development in industry in 2007. He holds 60 US patents.
INVITED TALK

10:35-11:05, October 9, 2019 Paper ID: 4079

Advances in Substrate Manufacturing for AI/HPC and 5G Packaging
Dr. Farhang Yazdani
President & CEO
BroadPak Corporation, USA

<Abstract>
Substrate is regarded as the foundation of semiconductor packaging. A substrate dictates overall form factor with first order effect on performance and cost of the finished product. Emerging heterogeneous chiplet integration, AI/HPC and 5G megatrends has created the need for advanced substrate technologies with superior performance and lower costs. With the industry embarking on heterogeneous integration of fine pitch devices there are even more pressure on end customers to manage fine bump pitch integration as well as performance and costs. We will present, emerging substrate technologies and manufacturing requirement for AI/HPC and 5G packaging.

.CV>
Farhang Yazdani is the President and CEO of BroadPak Corporation. BroadPak is internationally recognized as the “key provider of innovative total solution for 2.5D/3D products”. Through his 19 years with the industry, he has served in various technical, management, and advisory positions with leading semiconductor companies worldwide. He is the author of the book “Foundations of Heterogeneous Integration: An Industry-Based, 2.5D/3D Pathfinding and Co-Design Approach”. He is the recipient of 2013 NIPSIA award in recognition of his contribution to the advancement and innovations in packaging technologies. He has numerous publications and IPs in the area of 2.5D/3D Packaging and Assembly, serves on various technical committees and is a frequent reviewer for IEEE Journal of Advanced Packaging. He received his undergraduate and graduate degrees in Chemical Engineering and Mechanical Engineering from the University of Washington, Seattle.
**INVITED TALK**

15:00-15:30, October 9, 2019  
Paper ID: 4085

An Introduction to Marching Memory (MM)  
Prof. Tadao Nakamura  
Keio University  
Professor, Department of Information and Computer Science, Japan

<Abstract>

Today’s computer systems rather have a “big issue,” which is what is called the memory bottleneck, especially as their scale has been growing with nanotechnology year by year toward EXA-scale supercomputing for scientific calculations and deep learning in neural-networking. In modern computers, there exists mostly “serial data transfer” between memories and not random data transfer. Between HDD/Flash and DDRx-DRAM there is a page that is a group of bytes transferred as a single unit. Between DDRx-DRAM and caches, there is a cache line (line) that is a group of bytes transferred as a single unit. Even between a cache and a register file, the data transfer might be serial with cache lines. So, to drive existing computers faster with we introduce a new super memory “Marching Memory (MM).” The speed of MM is much faster than DRAM’s and even SRAM’s at lower power even though depending on applications. The feature of this is structurally speedup of accessing with high bandwidth and without delay. In case of MM, there is no addressing but it locates, without access protocols, an aimed memory location by data marching “column by column” within MM at a high speed. Thinking of all sorts of memories in general purpose computers, caches L1, L2 and L3 are the most suitable ones to be replaced with MM because these caches are constructed of SRAM that is not faster than MM and the power consumption is larger than MM’s. Especially in supercomputers the vector register could be replaced with MM, and a computer for deep learning expects high bandwidth with MM. As a result, MM could contribute to speedup of many computers with lower power.

<CV>

Tadao Nakamura received his PhD from Tohoku University in 1972. He was a Full Professor at Tohoku University from 1988 to 2007, and sent out internationally his many PhD graduates to universities and industries. He is a Professor Emeritus of Tohoku University, and also has been a Professor (as a visiting status) of Keio University since 2007. Especially in 1994 he was given the status of a Full Professor (Principal of Stanford Computer Architecture as a visiting status) in the Electrical Engineering Department at Stanford University. And even today he still stays at Stanford University at any time because he with Professor Michael J. Flynn has been creating the new concept of much higher speed memory with lower power consumption, named Marching Memory (MM), to avoid the memory bottleneck in computer systems. In 2007 he was also induced as a Professorial Fellow at Imperial College London. Meanwhile, as for lectures, he worked at Cambridge University in England, The University of Michigan, and The University of Tokyo in suitable positions such as a guest professor. His research interests are toward computer systems. In 2004 he received the IEEE Computer Society’s Taylor L. Booth Award. He has been Steering Committee Chair, after the Organizing Committee Chair and Advisory Committee Chair of COOL Chips conference series fully sponsored by the IEEE Computer Society. He is Life Fellow of the IEEE.
Future Challenges to Packaging Technologies of High Bandwidth Memory
Dr. Ho-Young Son
Principal Engineer, SK Hynix, Korea

<Abstract>
High bandwidth memory (HBM) is a new and an innovative solution satisfying with semiconductor industry trends representing as the era of big data and cloud computing. SK hynix HBM1, world 1st DRAM product released in 2013 opened up the new era in memory industry by showing the excellent performance in a view of lower power and higher bandwidth and the possibility to expand the memory capacity by multi-die stacking with through silicon vias (TSVs). Starting from the high speed graphic applications, HBM is now expanding its possible applications to high performance computing, network server, accelerators and other SoC and it promotes a lot of packaging technology challenges to meet the needs of semiconductor industry market.

Above all, capacity increase is one of the most important requirements for HBM. The increase not only in chip capacity but die stack count is strongly needed. However, increasing the number of stacked die is more preferable and realistic than chip capacity increase due to the limitation of transistor scaling and its poor effectiveness in chip size decrease. To adjust same die thickness with neighboring SoC die, HBM package thickness should be kept and its die thickness should be lower to achieve higher stack. Thin wafer and die handling technologies below 40um are complicated challenge in future HBM. Temporary wafer supporting system, damage-less thin die handling, and more precise die warpage control are needed. The increase in bandwidth accomplishes the increase in thermal designed power. Adding to higher stacked structure, thermal dissipation ability may get worse and it causes poor long-term transistor reliability by junction temperature increase. Power and thermal management would be a key factor to realize HBM3 or post HBM3. At the same time, a variety of package design rules should be shrunk. Finer TSV and micro-bump pitch and much narrower die-to-die gap have been continuously challenged conflicting many technical constraints. Consistent needs for both more capacity and higher bandwidth also drive another solution in system-in-package. The size limitation of a silicon interposer makes it difficult to adopt more HBM packages or larger SoC die. Si interposer can be replaced to organic interposer or RDL (redistribution layer) interposer. Direct attach of HBM to an organic substrate such as EMIB (embedded multi-die bridge) can be a good alternative to solve the size and cost problem of traditional silicon interposer technologies.

<CV>
Ho-Young Son received Ph.D in materials science and engineering at KAIST and has worked at SK Hynix since 2008. Now he is a principal engineer and in charge of wafer level package development such as 3D TSV, flip chip bump, fan out wafer level packages, and its process integration. Developed world first 8hi memory stack (2Gb*8hi) using TSV in 2011. Led HBM (high bandwidth memory) Gen1 development as the world first HBM product in 2013 and HBM2 in 2016 and 3DS DDR4 based 128GB LRDIMM (Load Reduced DIMM) in 2014 and implemented mass reflow processes for multi-die stacking in 2016. Now leading all of wafer level process development in SK Hynix including HBM2E and HBM3, which is upper version of HBM2, DDR5 3DS, cost effective RDL (redistribution) and CPB (copper pillar bump)/micro-bump technologies. Also he is looking for advanced technologies like homo- and heterogeneous stack solution of DRAM multi-die or DRAM/logic dies.
INVITED TALK

16:55-17:25, October 9, 2019 Paper ID: 4077
Monolithic 3D as an alternative to advanced CMOS scaling: technology, design and architecture perspectives
Dr. Pascal Vivet
Scientific Director
CEA-Leti, France

<Abstract>
Monolithic 3D technology (M3D) is a promising alternative to tackle the loss of Moore’s Law scaling beyond 22 nm node. By stacking different circuit layers thanks to nano-scale 3D Monolithic Inter Tier Via (MIV), it will be possible to offer a level of circuit integration never reached before, allowing advanced node scaling again as well as mixing heterogeneous technologies. M3D integrates sequentially different layers of transistors, with an ultra-fine pitch, in the 100 nm range, which is 200x smaller than state-of-the-art Through Silicon Vias (TSV) or 50x smaller than Copper to Copper Hybrid bonding (Cu-Cu HB). This high density 3D integration will pave the way towards new architectures, such as neuro- and bio-inspired applications, ultra-high density memory-computing cube and smarter mixed signal devices within tight low power constraints. This talk presents an overview of M3D technology and potential applications, and in more detail its associated design challenges, respectively on physical implementation aspects and on thermal dissipation.

<CV>
Dr. Pascal Vivet is Scientific Director of the Architecture, IC Design and Embedded Software Division in CEA-LETI, Grenoble, France. He received his PhD from Grenoble Polytechnical Institute in 2001, designing an asynchronous microprocessor. After 4 years within STMicroelectronics, he joined CEA-Leti in 2003 in the digital design lab. His research interests covers wide aspects of circuit and system level design, ranging from system integration, multi-core architecture, Network-on-Chip, energy efficient design, related CAD design aspects, and in strong links with advanced technologies such as 3D integration, Non-Volatile-Memories, photonics. He was project leader on 3D circuit design and integration since 2011. He participates to various TPC such as ASYNC, DATE, 3DIC conferences. He served as a member of the organizing committee of the 3D workshops series at DATE from 2013 to 2015, and to the D43D workshops since 2011. He has authored and co-authored more than 80 papers and holds several patents in the field of digital design. He co-authored a book chapter on “3D Integration in VLSI Circuits: Implementation Technologies and Applications.”
INVITED TALK

10:35-12:05, October 10, 2019 Paper ID: 4086
Future Directions for 3DIC Technology and Design
Prof. Paul D. Franzon
Cirrus Logic Distinguished Professor, Electrical and Computer Engineering, Director, Graduate Programs (EB2 3014B)
North Carolina State University (NCSU), USA

<Abstract>
3DICs have had major impact on memories and image sensors. What is next? First, we will make the case for memories with performance and power efficiency levels well beyond those of today. These will be largely driven by machine learning and artificial intelligence workloads. While the needs of convolutional neural networks can be met by HBM, other algorithms such as Multi-layer perceptron (MLP) and Long Short Term Memory require a lot more memory accesses per operation. Emerging cortically inspired algorithms, such as Hierarchical Temporal Memory, require even more bandwidth. We will describe some samples of what new memory architectures might look like and how their cost and performance are related to the underlying TSV technology.

Despite considerable research there have been little commercial takeup of logic on logic 3D chip stacks. This is despite the potential for logic on logic to help in scaling beyond that achieved by Moore’s Law alone. This potential will be realized as we approach the 5 nm node and hybrid bonding technology achieves its full potential. The case for 3D logic will be made based on a combination of technology push and cost-performance scaling pull. Chiplets integrated using interposers also have considerable potential for resulting in widespread 3D adoption. Results of recent experiments designing chiplets for machine learning will be presented along with anticipated results.

<CV>
Paul D. Franzon is currently the Cirrus Logic Distinguished Professor and the Director of Graduate programs in the Department of Electrical and Computer Engineering at North Carolina State University. He earned his Ph.D. from the University of Adelaide, Adelaide, Australia. He has also worked at AT&T Bell Laboratories, DSTO Australia, Australia Telecom, Rambus, and four companies he cofounded, Communica, LightSpin Technologies, Polymer Braille Inc. and Indago Technologies. His current interests include applying machine learning to EDA, building AI accelerators, neuromorphic computing, RFID, advanced packaging, 2.5D and 3DICs and secure chip design. He has lead several major efforts and published over 300 papers in these areas. In 1993 he received an NSF Young Investigators Award, in 2001 was selected to join the NCSU Academy of Outstanding Teachers, in 2003, selected as a Distinguished Alumni Professor, received the Alcoa Research Award in 2005, and the Board of Governors Teaching Award in 2014. He served with the Australian Army Reserve for 13 years as an Infantry Soldier and Officer. He is a pilot in the Bandit Flight Team, a formation flying unit. He is a Fellow of the IEEE.
INVITED TALK

13:30-14:00, October 10, 2019 Paper ID: 4084

Innovative bonding technology for 3D integration
Prof. Tadatomo Suga
Professor Emeritus of The University of Tokyo
Professor at Meisei University, Japan

<Abstract>
Effectiveness of the surface activation for room temperature bonding was demonstrated in the middle of '80, for example, for Al-Al and Al-Si3N4 in 1992, for Cu-Cu micro-bonding in 1993, and for the direct wafer bonding of Si-Si in 1996. The method is called as the surface activated bonding (SAB) and has been developed for heterogeneous bonding between different materials at room temperature, attracting increasing interest due to its simple process flow, no need for additional intermediate materials for bonding, and compatibility with CMOS technology. The standard SAB method is based on surface bombardment by Ar beam in ultra-high vacuum to clean the surfaces so that they can be bonded very strongly at room temperature without heat treatment. Modifications of the surface activation have been investigated to extend the standard SAB method for various materials and applications. The standard SAB method uses Ar beam bombardment to remove surface adsorption and oxidation layer to realize bonding between semiconductors when two surfaces are brought into contact. It has been studied for bonding of Si-Si, Ge-Ge, and compound semiconductors such as GaAs-Si. The standard SAB, however, failed to bond some dielectric materials, such as glass and silicon oxide. A modified SAB was developed to solve this problem, by using an intermediate layer of Si, metals, or even metal oxide deposited on the activated surfaces. The modified SAB is now applied to bond not only SiO2 glasses but also polymer films such as PEN and Polyimide, as well as WBG semiconductor wafers to diamond substrate with a wide perspective of the applicability on heterointegration for 3D, flexible and power electronics.

<CV>
Tadatomo SUGA joined the Max-Planck Institut fur Metallforschung in 1979, and received the Ph.D. degree in materials science from University of Stuttgart in 1983. Since 1984 he has been a faculty member of the University of Tokyo, and since 1993, he has been a professor at the Department of Precision Engineering of the School of Engineering. He was also the director of Research Group of Interconnect Ecodesign at National Institute of Materials Science (NIMS), and a Member of Japan Council of Science, as well as the chair of IEEE CPMT Society Japan Chapter. His researches focus on micro-systems integration and packaging, and development of interconnect technology, especially the room temperature bonding technique for 3D integration. He has endeavored to establish collaboration between industries and academia for the packaging technology, directing R&D project of the Institute of Micro-System Integration (IMSI), and advocating also importance of the environmental aspects of packaging technology as the key organizer of Japanese roadmap of lead-free soldering and International Eco-design Conference as well as the general chair of IEEE Workshop on Low Temperature Bonding for 3D integration. In March, 2019, he retired from the University of Tokyo, and joined Meisei University as a professor of the Collaborative Research Center on April 1. 2019. He became also an Emeritus Professor of the University of Tokyo on June 18. 2019.
INVITED TALK

15:15-15:45, October 10, 2019  Paper ID: 4082

Heat transfer in nanostructured Si and heat flux control technique

Prof. Masahiro Nomura
Associate Professor, Institute of Industrial Science
The University of Tokyo, Japan

<Abstract>
Heat transfer in Si nanostructure is not only an interesting topic in fundamental physics, but also an important practical study for efficient heat dissipation in electronic devices. In this talk, fundamentals of thermal phonon transport in nanostructured Si will be explained and some technique to control heat flux in Si membrane by nanostructuring will be introduced.

Heat dissipation is described by Fourier law in bulk material and the phonon transport is completely diffusive in this system. However, in micro/nano structures, where thermal phonon mean free paths are shorter than typical dimension of the structures, phonon transport will be semi-ballistic. In semi-ballistic phonon transport regime, thermal conductivity is no more intensive variable. Boundary or surface scattering processes determine the thermal conductivity of the system. In other words, nanostructuring can control the thermal conductivity of the material. For effective control of the thermal conductivity, the dimension of nanostructure should be designed by taking into account of thermal phonon spectrum of the material. Thermal phonons distribute to very broad frequency range, which corresponds to broad mean free path range. Therefore, it is essential to clarify the phonon mean free path spectrum and prepare nano/micro structures to impede the phonons in the volume zone. Thermal conduction reduction in well-designed poly-Si membranes with phononic crystal patterning will be introduced [1].

It is also interesting to develop heat flux control technique in Si by nanostructuring. We experimentally demonstrate formation of directional fluxes of ballistic phonons in one- and two-dimensional silicon phononic nanostructures, in which periodic arrays of nano-holes or corrugations formed directionality of the thermal phonons. This effect makes guiding and even focusing of heat fluxes possible in Si by nanostructuring [2, 3].


<CV>
Masahiro Nomura is Associate Professor in Institute of Industrial Science, The University of Tokyo. He received Ph.D. degree in Applied Physics in 2005, respectively, from The University of Tokyo. His research interests include hybrid quantum science, phonon/heat transport in semiconductor nanostructures, and energy harvesting by thermoelctrics. The concept of his current research is “from photonics to phononics” using phononic crystals, which have some physical analogy with photonic crystals. He is a recipient of The Young Scientists’ Prize by the Minister of Education, Culture, Sports, Science and Technology (2012), ISCS Young Scientist Award (2017), German Innovation Award – Gottfried Wagener Prize (2018), and ten other awards.
<Abstract>
Firstly I proposed to introduce a concept of 3D integration to DRAM and invented a 3D stacked capacitor DRAM cell in 1976 which has been widely used in the DRAM production. The stacked capacitor DRAM cell was the first commercialized 3D device. Various technologies and materials were integrated into the stacked capacitor DRAM cell which can be called a heterogeneous integration. This concept has been extended to a chip-level and wafer-level 3D integration using TSV in 1989. We succeeded in fabricating the first prototype 3DICs with a block parallel architecture using TSV, 3D stacked image sensor in 1999, 3D memory in 2000, 3D artificial retina chip in 2001 and 3D microprocessor chip in 2002. These early works succeeded to Japan national projects of JST brain project (1997-2002), NEDO dream chip project (2008-2013) and JST dependable VLSI project (2009-2014) where 3D neuromorphic chips, 3D stacked image sensor with extremely high frame rate of 10,000 frames/s and 3D multicore processor with self-test and self-repair function were developed. We have proposed a new heterogeneous 3D integration technology based on a self-assembly called a super chip for future 3D systems. In addition, we have been developing a 3D reconfigurable AI chip with a new cyclic architecture for future edge application.

<CV>
Mitsumasa Koyanagi received Ph.D. degree in electronic engineering from Tohoku University in 1974. Then he joined the Central Research Laboratory, Hitachi Ltd. where he worked on DRAM technology and invented a 3D stacked capacitor DRAM memory cell. He joined the Xerox Palo Alto Research Center, California in 1985 and Hiroshima University in 1988. He proposed 3D integration technology based on wafer-to-wafer bonding and Through-Si Via (TSV) in 1989. Since 1994, he has been a professor in Department of Machine Intelligent and Systems Engineering, Department of Bioengineering and Robotics, and currently New Industry Creation Hatchery Center (NICHe), Tohoku University where his interests are 3D integration technology, optical interconnection, nano-CMOS devices, memory devices, parallel computer system, neuromorphic devices and AI chip. He established the 3D LSI fabrication facility for 12-inch wafers, GINTI (Global Integration Initiative) in 2013. He was awarded IEEE Jun-ichi Nishizawa Medal, IEEE Cledo Brunetti Award, National Medal with Purple Ribbon in Japan, He is an IEEE life fellow. He is co-editor of Wiley’s “Handbook of 3D Integration”.
Fraunhofer has been working on 3D integration since end of 1980’s, when they successfully fabricated 3D CMOS devices based on recrystallization of Poly-Si. Then, in a cooperative project with Siemens we were the first to demonstrate a complete industrial 3DIC stacking process (1993-1996) based on wafer bonding and vertical integration of IC devices using inter-chip vias (later called TSV). Starting 1999, we investigated 3D TSV technologies with particular focus on die-to-substrate stacking and initiated the European Integrating Projects e-CUBES®, and e-BRAINS, where we evaluated the application of 3D heterogeneous integration, including demonstration of high-performance communications. In this paper we will also present ongoing developments in heterogeneous integration and approaches for systematic hierarchical modelling in order to carry out simulations in different physical domains, based on a unified description of the 3D system.

Peter Ramm is Head of Strategic Projects at Fraunhofer EMFT in Munich, Germany. He received Physics and Dr. rer. nat. degrees from the University of Regensburg and subsequently worked for Siemens in their DRAM facility in Regensburg, where he was responsible for the overall process integration with focus on backend-of-line. In 1988 he joined Fraunhofer IFT (now EMFT), working mainly on integration technologies for innovative devices and heterogeneous systems including the development of 3D TSV processes. Peter Ramm is co-author of over 100 publications and 36 issued patents (Europe, Japan, USA). He is IEEE Senior Member, IMAPS Fellow and Life Member, and received the Technical Achievement Award “For Pioneering Work on 3D IC Stacking and Integration” from IMAPS. Peter Ramm is co-editor of Wiley’s “Handbook of Wafer Bonding” and the series “Handbook of 3D Integration”.

13:20-13:30 Opening Ceremony

13:30-14:10 A1L-A, Plenary Talk I
Session Chair: Prof. Mitsumasa Koyanagi, Tohoku University

Paper ID: 4073
Presentation time: 13:30-14:10
On Why Dielets are the New Craze for Heterogeneous Integration
Subramanian S. Iyer
University of California, Los Angeles, United States
Abstract: Chiplets (or more accurately dielets) are the new thing in heterogeneous systems integration. In this talk, we will review why this makes sense and what the criteria for dielet selection are. Dielet selection depends on functionality and reuse potential but are constrained by yield, handling and testing. This limits the die size to between 1 and 100 mm2. The technologies that will be used to implement this concept are diverse and application dependent. They will require new substrate and assembly technologies. The dielet approach has significant challenges in both the infrastructure as well as the ecosystem. These include a secure supply chain and diversity of dielets. We’ll discuss those as well. We will introduce two heterogeneous integration platforms the SiIF and Flextrate to demonstrate these ideas. The dielet concept is gaining momentum and offers a good way to leverage the solid existing semiconductor infrastructure and make advanced packaging a much more value-add component of the technology.
Keywords: dielets chiplets, Heterogeneous Integration, Si, IF, Flextrate

14:10-16:05 A2L-A, Session 1: 3D Stacked Imager
Session Chair: Prof. Tetsu Tanaka, Tohoku University
Dr. Makoto Motoyoshi, Tohoku-MicroTec

Paper ID: 4078
Presentation time: 14:10-14:40
Invited Talk: 3D Integration Technologies For The Stacked CMOS Image Sensors
Yoshihisa Kagawa, Hayato Iwamoto
Sony Semiconductor Solutions Corporation, Japan
Abstract: Nowadays, the Internet-Of-Things (IoT) consists of a variety of LSIs. To use in different situations, small, multi-functional and high-performance LSIs have been strongly needed. One promising solution is System-In-Package (SiP) such as multi chip 2D package and 3D stack package. 3D chip stacking technology in particular can easily implement different function chips in a small system. We have contributed to the development of multifunctional, high-performance products with various 3D chip stacking technologies for many years.
Keywords: Back-Illuminated CMOS Image Sensor, Stacked CMOS Image Sensor, Cu-Cu Hybrid Bonding

14:40-14:55 Coffee Break

*Student Papers
**Abstract:** With the advent of the IoT era, more and more sensors are expected to be used in the future. The sensor needs an ADC that converts signals to digital values, but the sensor has different specifications such as signal bandwidth and dynamic range depending on the application. So far, ADCs of various conversion methods and performance have been developed according to the required specifications, but development efficiency is low, and development will be difficult if this is left as it is. Therefore, in this talk, we will discuss the possibility of ADC that can address many applications and required specifications with one ADC, while incorporating the latest technology trends.

**Keywords:** Sensor, Analog to Digital converter, Low energy, Wide dynamic range

**Paper ID:** 4018

**Presentation time:** 15:25-15:45

**Triple-Layering Technology for Pixel-Parallel CMOS Image Sensors Developed by Hybrid Bonding of SOI Wafers**

Masahide Goto¹, Yuki Honda², Toshihisa Watabe¹, Kei Hagiwara¹, Masakazu Nanba¹, Yoshinori Iguchi¹, Takuya Saraya³, Masaharu Kobayashi³, Eiji Higurashi⁴

¹NHK Science and Technology Research Laboratories, Japan; ²NHK Engineering System, Japan; ³The University of Tokyo, Japan; ⁴National Institute of Advanced Industrial Science and Technology, Japan

**Abstract:** We report a triple-layering technology for pixel-parallel CMOS image sensors. Photodiodes (PDs), logic circuits, and 16-bit pulse counters are developed on silicon-on-insulator (SOI) wafers, and they are three-dimensionally integrated within every pixel by using hybrid bonding through damascened Au electrodes of 5 μm in diameter in a SiO2 insulator. The developed triple-stacked wafers are confirmed to have no voids or separation of layers even after the removal of the handle layer, thereby demonstrating the feasibility of multi-layered imaging devices for the next-generation video systems.

**Keywords:** CMOS image sensors, three-dimensional integration, SOI, analog-to-digital converters
**Program Schedule – October 8, 2019 (Hotel Metropolitan Sendai)**

**14:10-16:05  A2L-A, Session 1: 3D Stacked Imager (continued)**

**Paper ID:** 4046  
**Presentation time:** 15:45-16:05  
**3D Integrated Pixel Sensor with Silicon-on-Insulator Technology for the International Linear Collider Experiment**  
Miho Yamada¹, Shun Ono², Yasuo Arai², Toru Tsuboyama², Masayuki Ikebe³, Makoto Motoyoshi⁴  
¹Tokyo Metropolitan College of Industrial Technology, Japan; ²High Energy Accelerator Research organization (KEK), Japan; ³Hokkaido University, Japan; ⁴Tohoku-MicroTec Co., Ltd., Japan  
**Abstract:** To implement high functional signal read out circuit in 20×20 μm² pixel, we designed chip-on-chip 3D integration pixel sensor for a vertex detector of the International Linear Collider experiment. Monolithic pixel sensor is processed by using fully-depleted silicon-on-insulator (FD-SOI) technology. 3D integrated chip consists of two SOI pixel sensor. Upper and lower chips are connected by Au micro cylinder bump bonding instead of generally used through silicon via (TSV). An analog and digital signal of lower pixel are sent to upper pixel via 3μm diameter of the bump. Response of the laser light of the first prototype 3D integrated chip called SOFIST4 was confirmed. It indicates that 3D integrated SOI pixel sensor has potential as the quantum imager.

**Keywords:** SOI, Monolithic pixel sensor, micro bump

**16:05-16:20  Coffee Break**

**16:20-17:50  A3L-A, Session 2: Integration Technology I**  
Session Co-Chairs: Prof. Chuan Seng Tan, Nanyang Technological University  
Dr. Murugesan Mariappan, Tohoku University

**Paper ID:** 4080  
**Presentation time:** 16:20-16:50  
**Invited Talk: Power-Performance Advantages of InFO Technology for Advanced System Integration**  
Chuei-Tang Wang, Douglas Yu  
Taiwan Semiconductor Manufacturing Company Limited, Taiwan  
**Abstract:** The power-performance advantages of the InFO technology from thin dielectric layers, fine RDL lines, 3D vertical interconnects and multi-chip integration on power integrity (PI), signal integrity (SI) and RF are studied and compared to those of organic substrate technology. For PI, the InFO with IPD (Integrated Passive Device) has 56% lower of system power delivery networking (PDN) impedance and 25% lower of the 1st voltage droop. For SI, a record high 10 Tbps/mm of bandwidth density is obtained by the submicron RDL on InFO. For RF system integration, a 3D solenoid inductor on InFO package is demonstrated.

**Keywords:** wafer level system integration (WLSI), InFO, IPD, PDN impedance, voltage droop, submicron RDL, bandwidth density, 3D solenoidal inductor, Q-factor, RF

*Student Papers*
PROGRAM SCHEDULE – October 8, 2019 (Hotel Metropolitan Sendai)

16:20-17:50  A3L-A, Session 2: Integration Technology I (Continued)

Paper ID: 4012*
Presentation time: 16:50-17:10
Investigation of Low Temperature Cu Pillar Eutectic Bonding for 3D Chip Stacking Technology
Yi-Chieh Tsai, Chia-Hsuan Lee, Kuan-Neng Chen
National Chiao Tung University, Taiwan

Abstract: In this study, a chip level Cu pillar to In/Sn pad thermocompression bonding (TCB) structure was investigated. After reaching the target bonding force and the melting point of the pad, the In/Sn pad was in its liquid phase for a short time and then quickly diffused into the Cu pillar, which demonstrates that Cu-solder bonding with low bonding temperature (150°C) and low bonding time (1 min) can be realized in atmospheric environment. These bonding results with good electrical performance and bonding quality show the potential of this chip level stacking process.

Keywords: Eutectic bonding, microbump, stacking, IMC

Paper ID: 4016
Presentation time: 17:10-17:30
Process Complexity and Cost Considerations of Multi-Layer Die Stacks
Dimitrios Velenis, Joeri De Vos, Soon-Wook Kim, Jaber Derakhshandeh, Pieter Bex, Giovanni Capuz, Samuel Suhard, Kenneth June Rebibis, Stefaan Van Huylenbroeck
imec, Belgium

Abstract: The increased requirements of data processing and reduced data latency has driven the demand for multi-layer 3D stacks for high performance systems and memory applications. In this paper, different approaches for multi-layer stacking are considered, including wafer-to-wafer (W2W) and die-to-die (D2D) stacking. The complexity of each approach is evaluated in terms of manufacturing cost and its impact on the stacked-system yield.

Keywords: 3D system, W2W stacking, D2W stacking, manufacturing cost, stacking yield

*Student Papers
Program Schedule – October 8, 2019 (Hotel Metropolitan Sendai)

16:20-17:50  A3L-A, Session 2: Integration Technology I (Continued)

Paper ID: 4041
Presentation time: 17:30-17:50
A Graph-Based Model of Micro-Transfer Printing for Cost-Optimized Heterogeneous 2.5D Systems
Robert Fischbach, Tilman Horst, Jens Lienig
Dresden University of Technology, Germany

Abstract: Micro-transfer printing (μTP) is a promising assembly technology that enables heterogeneous integration of dies originating from different wafers. It combines the advantages of pick-and-place in terms of flexibility with the advantages of wafer-level processing in terms of high throughput. For designers, however, it is hardly possible to make use of μTP’s cost savings capability without appropriate design support tools. We propose a cost model to calculate the unit cost for a heterogeneous system manufactured by μTP as well as a graph-based model to determine and optimize wafer utilization. This enables the design of cost-optimized heterogeneous systems manufactured by μTP.

Keywords: heterogeneous integration, micro-transfer printing, maximum independent set, wafer utilization, modeling, economical cost function

18:00-20:00  Banquet

*Student Papers
PROGRAM SCHEDULE – October 9, 2019 (Miyagino Ward Cultural Center)

08:45  Registration starts

09:00-09:40  B1L-B, Plenary Talk II
Session Chair: Prof. Paul D. Franzon, North Carolina State University

Paper ID: 4074
Presentation time: 09:00-09:40
Heterogeneous and 3D Integration at DARPA
Timothy M. Hancock¹, Jeffrey C. Demmin²
¹Defense Advanced Research Projects Agency, United States; ²Booz Allen Hamilton, United States
Abstract: Next generation electronic systems face the challenges of signal interconnect in an increasing dense fashion will use diverse technology sets that requires an unprecedented level of complexity at the board, package and chip level. This paper will focus on the problems facing the commercial and defense community and how DARPA investments in heterogeneous and 3D integration are tackling this challenge. Work from the Diverse Accessible Heterogeneous Integration (DAHI) program will be the primary focus and will highlight the use of dielet bonding and wafer-scale bonding of CMOS with InP, GaN and GaAs for use in wideband RF and mixed-signal systems. Some of the challenges and successes of integrating a diverse set of compound semiconductors will be presented.
Beyond DAHI, an overview of the Common Heterogeneous Integration and IP Reuse Strategies (CHIPS) program will be presented where the focus is on the reuse of CMOS dielet building blocks as an alternative to low-volume ASIC development. Finally, early work in the 3DSOC program will highlight how 3D monolithic integration may help break the memory wall at relaxed lithography nodes.
Keywords: Heterogeneous Integration, 3D Integration, RF and Mixed-Signal

09:40-10:20  B2L-B, Plenary Talk III
Session Chair: Dr. Peter Georg Ramm, Fraunhofer EMFT

Paper ID: 4075
Presentation time: 09:40-10:20
Quantum Annealing and its Application - New Generation of Natural Computing
Masayuki Ohzeki
Tohoku University, Japan
Abstract: Quantum annealing is a generic solver for optimization problems, which uses fictitious quantum fluctuation. The most groundbreaking progress in the research field of quantum annealing is its hardware implementation, that is, the so-called quantum annealer, by using artificial spins. In this presentation, we demonstrate several application of quantum annealing in real industry after a short introduction.
Keywords: Quantum annealing, optimization, machinelearning

10:20-10:35  Coffee Break at PatoNa Theater/Exhibition Hours

*Student Papers
PROGRAM SCHEDULE – October 9, 2019 (Miyagino Ward Cultural Center)

10:35-12:05  B3L-B, Session 3: Integration Technology II
Session Chair: Prof. Shoso Shingubara, Kansai University
Prof. Takafumi Fukushima, Tohoku University

Paper ID: 4079
Presentation time: 10:35-11:05
Invited Talk: Advances in Substrate Manufacturing for AI/HPC and 5G Packaging
Farhang Yazdani
BroadPak Corporation, United States

Abstract: Substrate is regarded as the foundation of semiconductor packaging. A substrate dictates overall form factor with first order effect on performance and cost of the finished product. Emerging heterogeneous chiplet integration, AI/HPC and 5G megatrends has created the need for advanced substrate technologies with superior performance and lower costs. With the industry embarking on heterogeneous integration of fine pitch devices there are even more pressure on end customers to manage fine bump pitch integration as well as performance and costs. We will present, emerging substrate technologies and manufacturing requirement for AI/HPC and 5G packaging.

Keywords: Substrate, AI, 5G, Packaging, Chiplet Integration

Paper ID: 4049*
Presentation time: 11:05-11:25
High density and low-temperature interconnection enabled by mechanical self-alignment and electroless plating
Sreejith Kochupurackal Rajan¹, Ming Jui Li¹, Gary May², Muhannad Bakir¹
¹Georgia Institute of Technology, United States; ²University of California, Davis, United States

Abstract: In this paper, we present and discuss the use of mechanical self-alignment in conjunction with metal electroless deposition as a method to facilitate low temperature, low pressure and high interconnect density inter-die bonding in heterogeneous 2.5D and 3D ICs. This method is a highly scalable alternative to the conventional solder-based interconnects but comes without the stringent requirements like including high temperature tolerance, high pressure process, extreme surface planarity and cleanliness requirement, and very accurate initial alignment of Cu-Cu direct bonding. The conjunction with mechanical self-alignment, which has demonstrated sub-micron alignment accuracies, also helps scale the pitch easily.

Keywords: Heterogeneous Integration, interconnects, electroless plating, self-alignment

*Student Papers
**Program Schedule – October 9, 2019 (Miyagino Ward Cultural Center)**

**10:35-12:05 B3L-B, Session 3: Integration Technology II (Continued)**

**Paper ID: 4013**  
**Presentation time: 11:25-11:45**  
**Design Considerations and Fabrication Challenges of Surface Electrode Ion Trap with TSV Integration**  
Jing Tao¹, Hong Yu Li², Peng Zhao¹, Yu Dian Lim¹, Anak Agung Alit Apriyana¹, Chuan Seng Tan¹  
¹Nanyang Technological University, Singapore; ²Institute of Microelectronics, Singapore  
**Abstract:** Surface electrode ion trap with through-silicon-via (TSV) integration enables 3D stacking of ion trap chip on an interposer to eliminate the wire-bonds on the surface electrodes and also addresses the challenge of the ever increasing complexity of surface electrode design with low-parasitic and high-density interconnect requirements. In this work, we demonstrate the design and fabrication of TSV integrated surface electrode ion trap on a 300-mm Si wafer platform. By designing the TSV arrays directly underneath the surface electrodes, the surface electrode footprint is reduced and the TSV traps show better RF performance compared to the planar traps with wire-bonding pads.  
**Keywords:** TSV, design and simulation, fabrication, ion trap, quantum computing

**Paper ID: 4011**  
**Presentation time: 11:45-12:05**  
**Fabrication and Morphology Analyses of Nano-Scale Interconnects for 3D-Integration**  
Murugsan Mariappan, Takafumi Fukushima, Hiroyuki Hashimoto, Jichel Bea, Mitsumasa Koyanagi  
Tohoku University, Japan  
**Abstract:** An advanced Directed-Self-Assembly (DSA) assisted vertical nano-scale interconnection formation is realized inside deep Si trench structures. Based on Flory-Huggins theory, nano-cylindrical structures with and without metal nano-particles were obtained for a nano-composite containing di-block co-polymer and metal nanoparticles. Low-temperature transmission electron micros-copy was primarily used to analyze the DSA-formed vertical nano-structures inside Si deep trenches.  
**Keywords:** Directed Self Assembly, nano-TSV, 3D

**12:05-13:30 Lunch Time/Exhibit Hours**

*Student Papers*
PROGRAM SCHEDULE – October 9, 2019 (Miyagino Ward Cultural Center)

13:30-15:00  B4P-C, Poster Session Core Time at PatoNa Theater

Paper ID: 4002*
Misalignment Analysis and Electrical Performance of High Density 3D-IC Interconnects
Imed Jani, Didier Lattard, Pascal Vivet, Lucile Arnaud, Beigné
CEA-LETI, France

Abstract: 3D integration is a promising solution to meet the increased need for functionality, density and performance of future integrated circuits. It is an attractive technique to address the requirements of several applications such as smart imagers, high-performance computing and memory-on-logic folding. However, test and characterization of such fine-grained 3D interconnect is still an open issue; Cu-Cu interconnects are prone to many structural defects due to fabrication process, such as misalignment, which needs to be thoroughly tested to ensure the performance of 3D-ICs. In this paper, the causes of local misalignment are well detailed. Then, a simulation using Matlab tool is illustrated and finally the impact of misalignment defect on resistance and capacitance parameters is demonstrated.

Keywords: 3D-IC, high density interconnects, Cu-Cu hybrid bonding, alignment, test vehicles

Paper ID: 4003*
Effects of Argon and Nitrogen Ion Bombardments on Sputtered and Electroplated Cu Surfaces for Cu Bonding Application
Han Kyeol Seo, Hae-Sung Park, Sarah Kim
Seoul National University of Science and Technology, Korea

Abstract: The comparative study of the formation of copper nitride on sputtered and electroplated Cu surfaces was studied through structural, chemical, and electrical analysis. Both sputtered and electroplated Cu thin films had the preferred orientation of (111) plane, but the sputtered Cu exhibited larger grains than the electroplated Cu. Based on the XPS analysis, the sputtered Cu formed more copper nitrides and fewer copper oxides than the electroplated Cu, which led to a significant improvement in bonding quality at the Cu bonded interface.

Keywords: Cu Bonding, Nitrogen Ion Bombardment, 3D Integration

Paper ID: 4004*
Characterization of Nitride Passivated Cu Surface for Low-Temperature Cu-Cu Bonding
Hae-Sung Park, Han Kyeol Seo, Sarah Kim
Seoul National University of Science and Technology, Korea

Abstract: A nitride passivated Cu surface has been investigated to improve Cu-Cu bonding quality bonded at 300°C. For an oxidation-free Cu surface, N2 plasma treatment was performed on CU surface followed by surface clean and activation by Ar plasma treatment. In this study, a response surface methodology in DOE was used for an optimized condition for a passivation formation. With low pressure and low RF power, the effects of the formation of copper nitride nitric and deoxidation were found to be better.

Keywords: Cu Bonding, Nitrogen Ion Bombardment, 3D Integration

*Student Papers
3:30-15:00  B4P-C, Poster Session Core Time at PatoNa Theater (Continued)

Paper ID: 4006
Tin Guard Ring Around TSV for Cross-Talk Suppression of Parallel Networking Lines of Data Center
Alit Apriyana Anak Agung, Zhao Peng, Chuan Seng Tan
Nanyang Technological University, Singapore

Abstract: This paper presents the design of TiN guard ring structure that is built around the through silicon via (TSV) to improve the signal integrity (SI) performance of parallel networking lines by suppressing the crosstalk from adjacent TSV. The guard ring enhances the insertion loss by up to 1.6 dB and the crosstalk isolation by 20 – 26 dB across a range of 0 – 40 GHz. The attainable data rate is higher than 50 Gbps under 50 Ohm load and higher than 10 Gbps under 1 pF capacitive loading. The obtained signal-to-noise ratio (SNR) is greater than 15.

Keywords: TSV, 3D Packaging, High Speed Digital, Interconnect

Paper ID: 4007*
Low-Temperature Wafer-Level Au-Au Bonding at 100 °C
Po-Chih Chen, Demin Liu, Kuan-Neng Chen
National Chiao Tung University, China; National Chiao Tung University, Taiwan

Abstract: In this work, gold is utilized as a thin film material to achieve low-temperature TCB at 100 °C. The gold thin film can reduce the copper bonding temperature and avoid the formation of IMCs. Additionally, gold has a lower hardness compared to copper, and surface roughness can be reduced with a gold thin film on the copper. The gold layer has high chemical stability and can protect the RDL from oxidation. These properties are helpful during the TCB process.

Keywords: low-temperature, wafer-level, bonding

Paper ID: 4008*
Low Temperature Cu-Cu Direct Bonding Below 150°C with Au Passivation Layer
Demin Liu, Po-Chih Chen, Yi-Chieh Tsai, Kuan-Neng Chen
National Chiao Tung University, Taiwan; National Chiao Tung University, China

Abstract: In this research, Au was proposed as a new passivation material for Cu-Cu direct bonding. According to TEM results, Cu can diffuse through the Au passivation layer to the bonding interface during the TCB process. In addition, the Au passivation layer can lower the bonding temperature (150 °C) and improve electrical properties compared to conventional Cu-Cu bonding, which is shown in the electrical measurement results. Furthermore, the electrical measurement results after reliability testing show that the Au passivation method is a reliable way to reduce the thermal budget of Cu-Cu direct bonding.

Keywords: Low-temperature, Wafer-level, Direct bonding

*Student Papers
PROGRAM SCHEDULE – October 9, 2019 (Miyagino Ward Cultural Center)

13:30-15:00  B4P-C, Poster Session Core Time at PatoNa Theater (Continued)

Paper ID: 4009*
Temperature Cycling Reliability of Wow Bumpless Through Silicon Vias
Chia-Hsuan Lee¹, Hsin-Chi Chang², Jui-Han Liu², Hiroyuki Ito¹, Young Suk Kim¹, Kuan-Neng Chen², Takayuki Ohba¹
¹FIRST, Tokyo Institute of Technology, Tokyo, Japan; ²Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan

Abstract: In this study, we investigated the temperature cycling reliability of bumpless through silicon vias (TSVs) using a wafer-on-wafer (WOW) process. TSV interconnects were fabricated with and without via bottom cleaning, and TCT tests were conducted under the same conditions. We examined how the cleaning process affected the temperature cycling reliability. In addition, self-aligned multiple TSVs were found to be a key feature of WOW bumpless TSVs. The impact of a multi-via structure on the temperature cycling reliability was investigated as well. The results show that the resistances of bumpless TSVs with via bottom cleaning and multiple TSVs exhibited better temperature cycling reliability.

Keywords: 3DIC, TSV, bumpless, wafer-on-wafer, interconnect

Paper ID: 4015
Protective Layer for Collective Die to Wafer Hybrid Bonding
Fumihiro Inoue¹, Julien Bertheau¹, Samuel Suhard¹, Alain Phommahaxay¹, Takuya Ohashi², Tetsuro Kinoshita², Yohei Kinoshita², Eric Beyne¹
¹imec, Belgium; ²Tokyo Ohka Kogyo Co., LTD, Japan

Abstract: Blade dicing compatible particle protective layers are assessed for collective Die-to-Wafer (D2W) direct bonding. Having the compatibility to blade dicing, the protective layer needs to be insoluble for de-ionized water (DIW), because blade dicing requires cooling water to maintain the cutting performance. Therefore, polymers soluble in alkaline solutions (e.g. TMAH, NH4OH) are tested for collective die to wafer direct bonding. With the dicing particle protective layer technologies, successful collective die to wafer direct bonding with current die assembly tools are achieved. The alternative protective layer ensures high yield and cost of ownership for collective die to wafer integration

Keywords: Collective D2W, Hybrid bonding, Dicing

Paper ID: 4017
Multichip CMOS Image Sensor Structure for Flash Image Acquisition
Yoshiaki Hagiwara
AIPS, Japan

Abstract: The important features of Buried Pinned Photodiode needed to build a new 3-D multichip flash image data acquisition system are explained. After in-pixel ADC, convention digital circuits can be applied. Buried Photodiode is suitable for the back light illumination scheme for the 3-D multichip system. Pinned Photodiode has the surface P+ hole accumulation (HAD) layer with the low dark current feature. The new mechanism of hole electron pair generation of Pinned Photodiode is explained. Photo electrons are separated from holes in the presence of the surface built-in potential barrier near the border of the surface P+ hole accumulation (HAD) layer.

Keywords: Image Sensor, Back Light Illumination, Stacked Chips

*Student Papers
**Paper ID: 4021**

Variability Cancellation to Improve Diagnostic Performance of Testing Through Silicon Vias in Power Distribution Network of 3D-IC

Koutaro Hachiya¹, Atsushi Kurokawa²

¹Teikyo Heisei University, ²Hirosaki University, Japan

**Abstract:** A novel method is proposed to improve diagnostic performance and to decrease probability of false diagnoses in testing open defects of TSVs in PDN of 3D-ICs. The conventional method measures resistances between micropumps placed exactly under TSVs and detects defects of the TSVs by changes of the resistances. But its diagnostic performance is not enough for practical applications. The proposed method measures resistance of another micropump pair to cancel the manufacturing variabilities in the conventional detecting resistance. Experimental simulation results show that the diagnostic performances of the proposed method reach the practical level.

**Keywords:** TSV, Open defect, Power distribution network, Design for test

**Paper ID: 4022**

Electrical Field Test Method of Resistive Open Defects Between Dies by Quiescent Currents Through Embedded Diodes

Hanna Soneda¹, Masaki Hashizume¹, Hiroyuki Yotsuyanagi¹, Shyue-Kung Lu²

¹Tokushima University, Japan; ²National Taiwan University of Science and Technology, Taiwan

**Abstract:** Dies in 3D stacked ICs are connected with Through-Silicon-Vias or micro bumps. Resistive open defects may occur at interconnects between the dies in fabrication process. The defects may grow to an open circuit fault in the field after shipping to a market. In this paper, a field test method is proposed so as the defect to be detected after shipping to a market. This test method is based on a quiescent supply current that is made flow through an interconnect. It is shown by Spice simulation that an increase of 0.01Ω is detected by the test method in field tests.

**Keywords:** Electrical interconnect test, Filed test, Resistive open defect

**Paper ID: 4023**

On Delay Elements in Boundary Scan Cells for Delay Testing of 3D IC Interconnection

Toshiaki Satoh, Hiroyuki Yotsuyanagi, Masaki Hashizume

Tokushima University, Japan

**Abstract:** For testing delay faults in 3D IC interconnection, we have proposed a DFT (Design-for-Testability) method for TSVs using a modified boundary scan circuit with embedded Time-to-Digital Converter (TDCBS). In this paper, for improving delay resolution, delay gates that have small propagation delay time have been investigated and implemented as a delay line. In order to prevent pulse shrinking of transition signal through a delay line, the proposed cell is designed to reduce the difference in transition delay between the delay for rising transition and falling transition. The measurement results for an experimental chip show the effectiveness of our new design.

**Keywords:** delay faults, post-bond testing, design-for-testability, boundary scan

*Student Papers*
PROGRAM SCHEDULE – October 9, 2019 (Miyagino Ward Cultural Center)

13:30-15:00  B4P-C, Poster Session Core Time at PatoNa Theater (Continued)

Paper ID: 4024
Growth Optimization of Multi-Layer Graphene for Thermal-TSV Application in 3D-LSI
Murugesan Mariappan, Takafumi Fukushima, Mitsumasa Koyanagi
Tohoku University, Japan

Abstract: A feasibility study for the continuous formation of multi-layer graphene (MLG) inside the TSV by thermal chemical vapor deposition technique was carried out. Both microstructural and micro-Raman investigations on the cross-sectional samples revealed the continuous formation of MLG all along the TSV for the growth temperature of 650°C and above, and it may be used as thermal TSVs for heat removal in the stacked tiers of 3D-LSI/IC.

Keywords: MLG, TSV, CVD

Paper ID: 4025*
Characterization of Low-Height Solder Microbump Bonding for Fine-Pitch Inter-Chip Connection in 3DICs
Yuki Miwa, Sungho Lee, Rui Liang, Kousei Kumahara, Hisashi Kino, Takafumi Fukushima, Tetsu Tanaka
Tohoku University, Japan

Abstract: We have fabricated microbump daisy chains with a low-height solder thickness of 2.5 µm in order to evaluate flip-chip bonding capabilities. Electrical characteristics of the bonded microbumps in three-dimensionally stacked chips were compared between a very thin non-conductive film (NCF) and capillary underfill (CUF). The resulting I-V behaviors showed that the resistance of the daisy chain with the NCF was lower than that with the CUF, indicating that the low-height solder microbumps with combination of the thin NCF can be a promising candidate for future fine-pitch inter-chip connection in 3DICs.

Keywords: Microbump, 3DIC, NCF, Flip-chip bonding

*Student Papers
**Program Schedule – October 9, 2019 (Miyagino Ward Cultural Center)**

**13:30-15:00  B4P-C, Poster Session Core Time at PatoNa Theater (Continued)**

**Paper ID: 4026**  
**Development of Laser-Assisted Bonding with Compression (LABC) Process for 3D IC Integration**
Kwang-Seong Choi, Yong-Sung Eom, Seok Hwan Moon, Jiho Joo, Kwangjoo Lee, Jung Hak Kim, Ju Hyeon Kim

1ETRI, Korea; 2LG Chem, Korea

**Abstract:** Laser-Assisted Bonding with Compression (LABC) technology with NCF was proposed to accomplish the productivity and process reliability at the same time. A quartz block as a header was used to deliver a pressure to the devices because of its extremely low absorption of the laser during the bonding process. Newly developed NCF for LABC was designed not only to be applicable to the conventional TCB technology but also to have stability on a hot stage and to show solder wetting and fast curing with no void and optimal fillet during the LABC bonding process. As the laser power is used as a heat source, the uniform heat should be provided on each interconnection without any damages on a substrate. 780 μm-thick daisy chain top and bottom chips with the minimum pitch of 30 μm and bump number of about 27,000 were successfully bonded using the LABC and NCF film.

**Keywords:** Laser-Assisted Bonding with Compression, NCF, throughput, fine-pitch interconnections,

**Paper ID: 4028**  
**A Built-in Self-Test Scheme for TSVs of Logic-DRAM Stacked 3D ICs**
Wei-Hsuan Yang, Jin-Fu Li, Chun-Lung Hsu, Chi-Tien Sun, Shih-Hsu Huang

1National Central University, Taiwan; 2ITRI, Taiwan; 3Chung Yuan Christian University, Taiwan

**Abstract:** Three-dimensional (3D) dynamic random access memory (DRAM) using through-silicon-via (TSV) has been proposed to overcome the memory wall. WideIO DRAM is one of 3D DRAMs. IOs of a WideIO DRAM die are wrapped by a 1149.1-like boundary scan controlled by a scan controller. In this paper, we propose a built-in-self-test (BIST) scheme for the postbond testing of TSVs of a logic-DRAM stack. The BIST circuit implemented in the logic die can generate control signals for the scan controller and test patterns for the testing of TSVs.

**Keywords:** 3D IC, TSV, post-bond test, BIST
**Paper ID: 4029**
Cu diffusion barrier properties of various CoWB electroless plated films on SiO2/Si substrate for via-last TSV application
Taro Matsudaira¹, Shunsuke Shindo¹, Kosei Morita¹, Tomohiro Shimizu¹, Takeshi Ito¹, Shoso Shingubara¹, Satoru Shimizu²
¹Kansai Univ., Japan; ²JCU Corporation, Japan

**Abstract:** There is a serious problem of poor sidewall coverage for the sputtered barrier metals in high aspect ratio TSVs, and it is becoming difficult for complete filling of Cu. We have proposed electroless plated Co-alloy barrier metals for replacing conventional sputtered barrier metals. In this study, we evaluated Cu diffusion barrier properties of various electroless CoWB films with different atomic compositions. CoWB and CoB films were electroless plated on Pd nanoparticle catalyst. A typical structure for evaluation of interdiffusion is stacked layers of TiN/Cu/CoWB barrier layer/thin SiO2/Si substrate. We evaluated Cu interdiffusion characteristics after annealing by SIMS depth profiling. The ratio of the atomic composition of CoWB were varied by tuning plating bath conditions. It was shown that an electroless CoWB film with W content larger than 15% had a good Cu diffusion barrier property against 350°C annealing.

**Keywords:** TSV, Cu diffusion, XPS, SIMS

**Paper ID: 4030**
Photoresist Development for wafer-Level Packaging Process
Makiko Irie
Tokyo Ohka Kogyo Co., LTD, Japan

**Abstract:** Semiconductor assembly process has been improved by wafer level packaging (WLP) introduction in high volume manufacturing. Cu Redistribution layer (RDL) miniaturization is one of key process for small, thin and light chip manufacturing. Development of high resolution and transmittance control of photoresist is required to this technology realization on topology substrate. Photoresist development with high resolution and transmittance is required to this technology realization on the topology substrate. Chemical amplified (CA) type photoresist indicated stable sensitivity at various thickness because of high transparency at 365 nm wavelength. Below 2 μm L&S resolution was achieved by the optimized formulation in this research.

**Keywords:** photolithography, photoresist, NQD, CA, ultra-fine-pitch
13:30-15:00  B4P-C, Poster Session Core Time at PatoNa Theater (Continued)

Paper ID: 4031
SiN used as a stressor in Germanium-On-Insulator substrate
Sethavut Duangchan¹, Keisuke Yamamoto², Dong Wang², Hiroshi Nakashima³, Akiyoshi Baba⁴
¹Department of Industrial Physics and Medical Instrumentation, King Mongkut’s University of Technology, Thailand; ²Interdisciplinary Graduate School of Engineering Sciences, Kyushu University, Japan; ³Global Innovation Center, Kyushu University, Japan; ⁴Center for Microelectronic Systems, Kyushu Institute of Technology, Japan

Abstract: This research aims to show the advantage of using silicon nitride as a stressor in a strained germanium-on-insulator substrate. A Si substrate is patterned on the surface before bonding for controlling the bucking part, whereas the SiN film is deposited on Ge substrate by PE-CVD. Two wafers, Si and SiN/Ge are brought together by surface-activation bonding with 200 degree Celsius post-anneal. It was found that the tensile strain of 1.16% for the flat part and 2.03% for the bucking part, which is higher than other reported GOI using SiO2 layer.

Keywords: Strained-Ge, GOI, SiN, wafer bonding

Paper ID: 4032
Microstructural and Light Exposure Effects on Direct Copper to Copper Bonding
Zong-Yu Xie¹, Pin-Kuan Li¹, Jenn-Ming Song¹, David Tarng², Chih-Pin Hung²
¹National Chung Hsing University, Taiwan; ²Advanced Semiconductor Engineering Group, Taiwan

Abstract: This study aims to investigate microstructural and light exposure effects on direct Cu bonding. Electro-deposited Cu samples with different grain sizes, preferred orientations as well as hardnesses were prepared. The influence of individual factors will be studied especially grain size. Experimental results show that through grain refinement the strength of directly-bonded electroplated copper joints can be effectively increased by 30%. With an additional electromagnetic irradiation on the faying surface, the joint strength obtained is 129% higher than that of electroplated Cu bumps with coarse equiaxed grains.

Keywords: Electrodeposited Copper, Xenon Flash, grain boundary, texture

Paper ID: 4034
Electrostatic Shield TSVs to Suppress Coupling Among Stacked ICs
Yuuki Araga, Katsuya Kikuchi, Masahiro Aoyagi
National Institute of Advanced Industrial Science and Technology (AIST), Japan

Abstract: Multi chip modules (MCMs) employing three-dimensionally stacked ICs (3DS-ICs) are expected to be the integration method to achieve high performance by integrating memories and processors densely. In such a densely assembled modules, crosstalk between closely placed 3DS-ICs like a stacked memories and processors. In this study, we propose a shielding method using through silicon vias (TSVs) to suppress stack-to-stack crosstalk. we created MCM model for 3-D electromagnetic solver and simulated result showed good noise suppression effect. simulation result also showed higher suppression ratio as larger number of stacked ICs.

Keywords: TSV, Electrostatic Shield, MCM
13:30-15:00  B4P-C, Poster Session Core Time at PatoNa Theater (Continued)

Paper ID: 4035
Development of a CDS Circuit for 3-D Stacked Neural Network Chip Using CMOS Analog Signal Processing
Koji Kiyoyama¹, Qian Zhengy², Hiroyuki Hashimoto², Hisashi Kino², Takafumi Fukushima², Tetsu Tanaka², Mitsumasa Koyanagi²
¹Nagasaki Institute of Applied Science, Japan; ²Tohoku University, Japan

Abstract: The human brain is a highly parallel asynchronous network composed of hundreds of billions of nodes with multi-layered structure. Most of neuro chips have implemented a neural network system functions using two-dimensional chip and these chips have achieved great results. To realize low-power and multi-layered neuro chip that mimics the structure of the human brain, we have proposed a highly parallel analog signal processing method with three-dimensional (3D) stacked neural network system. The conceptual diagram of the 3-D stacked neural network system is illustrated in Fig. 1. The proposed 3-D stacked system consists of multiple layers of neuron chips for product-sum operation and SRAM memory chips for storing weight data. In this paper, we focus on a noise reduction technique that degrades the accuracy of the analog signal processing. The proposed noise reduction technique features low power and a small area and could be a novel solution for the deep neural networks (DNN) chip using analog signal processing method.

Keywords: 3D stacked Neuron Chip, CDS circuit, CMOS analog signal processing, AI chip

Paper ID: 4036*
Study of macEtch Using Additives for Preparation of tsv
Shunsuke Hanatani, Takuya Yorioka, Tomohiro Shimizu, Takeshi Ito, Shoso Shingubara
Kansai University, Japan

Abstract: Preparation of vertical and deep holes in Si (100) substrates for TSV application was demonstrated using a wet chemical process, which was metal-assisted chemical etching (MacEtch) of Si, instead of traditional dry etching process. Moreover, the effect of polarity of additives in the etching solution on the morphology of etched Si were investigated. Benzalkonium chloride (BKC), sodium lauryl sulfate (SLS) and polyethylene glycol (PEG), which were anionic, cationic and non-polar surfactant, respectively, were added into the etching solutions. It is found that the addition of surfactants in the etching solution improves etching morphology of Si, regardless of polarity of surfactants.

Keywords: si, wet etching, polarity of surfactant, 3d-lsi

*Student Papers
Paper ID: 4038
Reduction of TSV pumping
Quy Dinh¹, Kazuo Kondo¹, Tetsuji Hirato²
¹Fine Feature Electrodeposition Research Laboratory, Japan; ²Kyoto University, Japan
Abstract: The mismatch in thermal expansion coefficient (TEC) between copper and silicon causes serious problems in three-dimensional (3D) packaging. The common problem is TSV pumping when TSV is exposed to high temperature (400°C-600°C) during the wiring process. The copper pumping destroys wiring above TSV and leads to the failure of electronic devices. Other problem is the area on silicon around the TSV where the transistors cannot be formed due to stress caused by copper when annealing. With our low TEC additive (additive A), copper pumping height in 5x 20 µm p-TEOS TSV was reduced to 0.5 µm from 2.0 µm in case of conventional copper. We also investigated the effect of polyimide which is used as liner layer in the TSV on copper pumping reduction. The first screening result showed that the pumping height of conventional copper in polyimide TSV was only 0.8 µm., compared to 2.0 µm pTEOS TSV and 1.2 µm O3-TEOS TSV.
Keywords: TSV, Copper, Electrodeposition, TCE

Paper ID: 4040
3D Test Wrapper Chain Optimization with I/O Cells Binding Considered
Fan-Hsuan Tang¹, Hsu-Yu Kao¹, Shih-Hsu Huang¹, Jin-Fu Li²
¹Chung Yuan Christian University, Taiwan; ²National Central University, Taiwan
Abstract: Previous 3D test wrapper chain synthesis algorithms do not consider the binding of I/O cells (i.e., the association between scan chains and I/O cells). However, the binding of I/O cells may be specified as synthesis constraints. In this paper, we propose a 3D test wrapper chain optimization algorithm with I/O cells binding considered. Our objective is not only to reduce the required test time but also to reduce the number of test TSVs (through-silicon-vias) under I/O cells binding constraints. Our experiments show that the proposed algorithm greatly reduces both test time and test TSV count.
Keywords: Test Time, TSV Count, Test Wrapper Chain Synthesis, Test TSV, Optimization Algorithm
PROGRAM SCHEDULE – October 9, 2019 (Miyagino Ward Cultural Center)

13:30-15:00  B4P-C, Poster Session Core Time at PatoNa Theater (Continued)

Paper ID: 4043
**Cu-Cu Bonding Challenges with i-ACF® for Advanced 3D Integration**
Shunji Kurooka¹, Yoshinori Hotta¹, Ai Nakamura², Mitsumasa Koyanagi², Takafumi Fukushima²
¹FUJIFILM Corporation, Japan; ²GINTI, Japan

**Abstract:** In this work, we demonstrate ultrafine-pitch Cu-Cu interconnection with an inorganic anisotropic conductive film (i-ACF®). It consists with 60nm-diameter micro pores of anodic aluminum oxide film filled with copper. Lower-temperature/pressure Cu-Cu bonding below 250°C/50MPa have been achieved. When we employ a daisy chain consisting of 5,096 Cu electrodes with a size of 28 μm, the resulting resistance of each joint is found to be 0.1 Ω. The key process is Cu-Cu bonding through the i-ACF under a reducing atmosphere, which inhibits the oxidation of the Cu nano-pillars. The bonding temperature can be lowered down to 200°C.

**Keywords:** 3D integration, Direct bonding

Paper ID: 4044
**Study of Optimizing Stress-Strain Curve of Adhesive for High Expansion Tape**
Tadatomo Yamada, Ken Takano, Toshiaki Menjo, Shinya Takyu
LINTEC Corporation, Japan

**Abstract:** We have proposed a novel pick-up and place process for FO-WLP using high expansion tape and tape expansion machine device. In this study, the effect of stress-strain curve of adhesive for expansion tape is investigated. As a result of evaluation, average chip distance increases to 2,930 μm (initial chip distance; 35 μm) with 3 mm square chips and the standard deviation is 43 μm. We indicated that both properties of chip distances and chip accuracies can be achieved by using our expansion tape and machine device.

**Keywords:** FO-WLP, pick up and place, tape expansion

Paper ID: 4045
**Design of a 16kb SRAM in 3D Monolithic CoolCube technology**
Adam Makosiej¹, Pablo Royer², Francois Andrieu¹, Sebastien Thuries¹, Pascal Vivet¹, Edith Beigne¹
¹CEA-LETI, Minatec Campus, Univ. Grenoble Alpes, France; ²STMicroelectronics, France

**Abstract:** This paper describes, for the first time, a silicon implementation of the 16kB SRAM in 3D Monolithic CoolCube technology. The memory is split with memory bitcell array placed in the upper silicon tier and all peripheral logic placed in the bottom under the array. Two 3D SRAM implementations are presented showing a 40% are gain in respect to the reference 2D SRAM. The 3D design contains 98304 transistors in top tier (cold process) and 2064 Monolithic Inter-tier Vias (MIVs). Word-based redundancy block is implemented in the bottom silicon tier allowing correction of random faulty bits at low energy cost.

**Keywords:** Monolithic 3D, SRAM, Coolcube

*Student Papers*
PROGRAM SCHEDULE – October 9, 2019 (Miyagino Ward Cultural Center)

13:30-15:00  B4P-C, Poster Session Core Time at PatoNa Theater (Continued)

Paper ID: 4048*
Development of 3D-IC Embedded Flexible Hybrid System
Sungho Lee, Yuki Susumago, Zhengyang Qian, Noriyuki Takahashi, Hisashi Kino, Tetsu Tanaka, Takaumi Fukushima
Tohoku University, Japan
Abstract: We have fabricated a new 3D-IC embedded flexible hybrid system (FHS) based on a Fan-Out Wafer-Level Packaging (FOWLP). The unique FHS structure is consisting of PDMS as a flexible substrate in which the 3D-IC with through-Si vias (TSVs) and microbumps are embedded. The mechanical and electrical properties of the 3D-IC embedded FHS are characterized by using repeated bending test with the TSV/microbump daisy chains. The new FHS can be expected to be used as high-performance wearable device systems for biomedical applications.
Keywords: Flexible hybrid electronics (FHE), TSV

Paper ID: 4052
Optical TSV Using Si-Photonics Integrated Curved Micro-Mirror
Akihiro Noriki1, Isao Tama2, Yasuhiro Ibusuki2, Akio Ukita2, Satoshi Suda1, Daisuke Shimura2, Yosuke Onawa2, Hiroki Yaegashi2, Takeru Amano1
1National Institute of Advanced Industrial Science and Technology, Japan; 2Photonics Electronics Technology Research Association, Japan
Abstract: Optical through Si vias (TSVs) for Si photonics have been studied for many new applications and grating couplers have been used as vertical optical I/O (input/output) devices. Recently, we demonstrated a new vertical optical I/O using an integrated curved micro-mirror. Compared to grating couplers, broadband optical I/O can be available. In this work, a feasibility study of an optical TSV using the curved micro-mirror was carried out. A curved micro-mirror for an optical TSV of Si interposer up to 200-micrometer thickness was integrated on a Si photonics chip and the vertical optical output from the Si waveguide was demonstrated.
Keywords: Optical TSV, Si photonics, Mirror, Broadband

Paper ID: 4053
A Design Scheme for 3-D Stacked CNN Accelerators
Jubee Tada1, Kazuto Takahashi1, Ryusuke Egawa2
1Yamagata University, Japan; 2Tohoku University, Japan
Abstract: This paper proposes a design scheme of the module for a 3-D stacked convolutional neural network accelerator, which consists of several half-precision floating-point fused multiply-add units and weight register-files. The proposed scheme achieves up to a 10% power consumption reduction compared to a 2-D implemented module when the number of units and register-files is sixteen and the number of layers is two.
Keywords: 3D Design

*Student Papers
PROGRAM SCHEDULE – October 9, 2019 (Miyagino Ward Cultural Center)

13:30-15:00  B4P-C, Poster Session Core Time at PatoNa Theater (Continued)

Paper ID: 4054
X-ray photon-counting Imager with CdTe/Si-LSI stacking
Toru Aoki¹, Katsuyuki Takagi², Toshiyuki Takagi¹, Hiroki Kase¹, Akifumi Koike¹
¹Shizuoka University, Japan; ²ANSeeN Inc, Japan

Abstract: We have been developing CdTe based photon-counting X-ray/gamma-ray sensors and imagers. Several ten years ago, the pixel pitch was about 1 mm or 2 mm, so we could apply conventional wire-bonding technique. Nowadays, the pixel pitch is decreased to 100µm or less, so we cannot use wire-bonding technique and so on. Moreover, the signal processing of X-ray imager was changed from integrated scanning circuit (like a conventional CMOS or CCD for visible wavelength) to photon-counting at each pixel. Every pixel needs large scale signal processing circuit such as pre-amplifier, analog-digital converter, memory, data-transfer etc. Therefore, we designed this photon counting ASIC by using 0.13 µm-design rule and every pixel has the circuit as Shown in Fig. 2. In this study, the pixel pitch is 80 µm and data-bus pad was aligned at edges of ASIC, and we use TSV connection to master silicon substrate (up to 300 mm-diameter size) as shown in Fig. 1. The size of CdTe single crystal has limit (not so larger) and very weak material. So, we tiled CdTe/Si-LSI stacking chip on Si master substrate and signals are joined in Si master substrate as shown in Fig. 3. We also try to use super inkjet technology printer for making the bump-material. We have to put bumpmaterial on 80 µm pitch electrode on pads of Si-ASIC and connect to CdTe sensor pads. The silver-based ink was used for making these bumps and connect by using flip-chip-bonder.

Keywords: CdTe/Si-LSI stack, Hetero 3D, X-ray imager

Paper ID: 4055*
Transformer-less Floating Gate Driver for 3D Power SoC
Minami Nakayama¹, Seiya Abe², Satoshi Matsumoto²
¹Graduate School of Kyushu Institute of Technology, Japan; ²Kyushu Institute of Technology, Japan

Abstract: Power supply on chip (power-SoC) has been caught attentions because miniaturize the power supplies. Especially, the 3D power-SoC is attractive and is fabricated using LSI and MEMS process. It is important to meet the various electrical requirements for expanding applications because they are fabricated using mass production process. In such situations, series and/or parallel connections of them is attractive. However, we generally use transformers as power supplies for floating gate driver circuits when we connect DC-DC converters series. Transformers are not suitable for power-SoC because they disturb miniaturization. In this paper, we propose a transformer-less floating gate driver circuit for 3D power SoC.

Keywords: Power supply on chip, 3D power SoC, ISOP converter, Gate driver

*Student Papers
Program Schedule – October 9, 2019 (Miyagino Ward Cultural Center)

13:30-15:00 B4P-C, Poster Session Core Time at PatoNa Theater (Continued)

Paper ID: 4056
Investigation of the Influence of Material Properties on Warpage and Solder Joint Reliability of 2.5D & FO Package
Koji Hamaguchi, Mitsuki Nakata, Kouta Segawa, Naoya Suzuki, Toshihisa Nonaka
Hitachi Chemical Co., Ltd, Japan
Abstract: 2.5D and fan-out (FO) package have been one of the major research topics recently. In this paper, the warpage and the solder joint reliability of them were investigated using FEM by comparing with flip chip package. The results revealed that 2.5D structure showed the largest warpage and the least solder joint reliability among them. FO package showed that the minimum warpage and the maximum reliability.
Keywords: 2.5D, FO, Warpage, Reliability

Paper ID: 4057*
Design and Evaluation of a Novel and Ultra-compact Fully-TGV-based Self-shielding Bandpass Filter for 5G Applications
Ziyue Zhang¹, Yingtao Ding¹, Zhiming Chen¹, Mingrui Zhou¹, Miaoyiong Lei Xiao¹, Ziru Cai¹, Xiaogong Xia⁴
¹Beijing Institute of Technology, China; ²National University of Singapore, Singapore
Abstract: An ultra-compact bandpass filter (BPF) based on through-glass-via (TGV) technique is proposed. The BPF is composed of TGV-based 3D array capacitors and 3D spiral inductors. The fabrication flow is simple and the device area is extremely minimized thanks to the identical TGVs used in the BPF. Besides, a TGV-based shielding ring is utilized to elevate the anti-interference property of the BPF, which also optimizes the thermal dissipation capability. Scattering parameters of the BPF and heat dissipation property of the shielding ring are simulated and discussed. The BPF is promising for the minimization of future 5G applications and system integration.
Keywords: Bandpass filter, 3D integration, TGV, Minimization

Paper ID: 4058*
Impacts of Deposition Temperature and Annealing Condition on Ozone-Ethylene Radical Generation-TEOS CVD SiO2 for Low-Temperature TSV Liner Formation
Rui Liang, Sungho Lee, Yuki Miwa, Kousei Kumahara, Mariappan Murugesan, Hisashi Kino, Takafumi Fukushima, Tetsu Tanaka
Tohoku University, Japan
Abstract: Through-silicon vias (TSVs) is one of the key technologies for 3D integration. To solve the issues induced by the high-temperature process for TSV liner formation in the multichip-to-wafer (MCTW) process, we applied the low-temperature SiO2 deposition method, which called OER (Ozone-Ethylene Radical generation)-TEOS-CVD. In this study, we fabricated the MIS capacitors with the TSV liner deposited by OER-TEOS-CVD at 150°C and RT, and compared both coverage and electrical characteristics with that formed by conventional PE-CVD at 200°C. Furthermore, we analyzed these SiO2 liners by FTIR and synchrotron XPS. These results show OER-TEOS-CVD has great potentials to realize high-reliability TSVs and to apply to various processes in 3D integration.
Keywords: TSV, low-temperature process, CVD

*Student Papers
**Program Schedule – October 9, 2019 (Miyagino Ward Cultural Center)**

**13:30-15:00**  
**B4P-C, Poster Session Core Time at PatoNa Theater (Continued)**

**Paper ID: 4059**  
**Hydrolysis-Tolerant Hybrid Bonding in Ambient Atmosphere for 3D Integration**  
Akitsu Shigetou¹, Tilo Hongwei Yang², Robert Kao²  
¹National Institute for Materials Science, Japan; ²National Taiwan University, Taiwan

**Abstract:** In this study, a heterogeneous bonding between organic and inorganic materials was realized at low temperature without vacuum atmosphere, by means of the vapor-assisted vacuum ultraviolet (VUV) surface modification method. In this method, an ultrathin bridge layer was created between the surfaces via the VUV irradiation in nitrogen atmosphere containing lower alcohol vapor. The radical species of H, OH, and CH sequentially enabled the initial surface cleaning, partial deoxidization of native oxide, and the formation of hydroxyl-terminated alkyl bridge with multidentate carboxylate on the inorganic material. Due to the dynamic competition of reversible hydrolysis of the multidentate carboxylate, the waterproof characteristic was expected to the bridge layer. The bridge layer was then bonded strongly to the modified organic material surface by hydrogen bond on the moment of contact at room temperature, which was followed by the dehydration condensation upon heating at 423.2 K around. Given polyether ether ketone (PEEK) and wiring metals as the typical materials in the fields of flexible electronics and structural materials, the evolution of chemical surface binding condition was analyzed to optimize the bridge formation. The bond interface showed cohesive fracture after the high humidity storage testing at 358.2 K and RH 85% for 1000 hours. Such the hybrid bonding with ultrathin bridge layer will be of the actual use in 3D flexible integration in near future.

**Keywords:** hybrid bonding, low temperature, VUV

**Paper ID: 4062**  
**Stacked Pixel Sensor / Detector technology using Au micro-bump Junction**  
Makoto Motoyoshi, Koki Yanagimura, Taiko Fushimi, Shunta Endo, Motoki Kobayashi, Hideaki Tamate  
Tohoku-MicroTec Co., Ltd, Japan

**Abstract:** This paper presents the experimental results of a pixel detector device fabricated with 2.5-μm gold cone bump connections for checking the process integrity and Stacked heterogeneous X-ray sensor TEG with gold cylindrical bumps. And the stacked chip repairing technique using μ-bump bonding is presented.

**Keywords:** micro-bump, Pixel Sensor
**Paper ID: 4064**  
**Photoelectroscopic Study of Mn Barrier Layer on SiO2 for Si Wafer Bonding Process**  
Takahiro Nagata¹, Kazumichi Tsumura², Kenro Nakamura², Kengo Uchida², Jin Kawakita¹, Toyohiro Chikyow¹, Kazuyuki Higashi²  
¹National Institute for Materials Science, Japan; ²Toshiba corporation, Japan  
**Abstract:** The chemical bonding state of Mn film on SiO2, which is expected to be applied as a bonding material for Si wafer, was investigated by x-ray photoelectron spectroscopy (XPS). The as deposited Mn film had unintentionally oxidized surface and interface layer, caused by an air exposure and a redox reaction with SiOx at the SiO2 surface, respectively. Post deposition anneal (PDA) enhanced the redox reaction between MnOx and SiO2. The N2 plasma treatment eliminates the redox reaction, and enhances the Si-Mn-O bonding formation, which should improve the tensile strength of wafer bonding.  
**Keywords:** Direct bonding

**Paper ID: 4065**  
**Crystallinity Dependence of Long-Term Reliability of Electroplated Gold Thin-Film Interconnections**  
Ken Suzuki, Ryota Mizuno, Yutaro Nakoshi, Hideo Miura  
Tohoku University, Japan  
**Abstract:** The effect of crystallinity in electroplated gold thin-film interconnections on their electromigration (EM) resistance was investigated experimentally. The activation energy in Black’s equation was evaluated by accelerated EM tests and Arrhenius plot as a function of the crystallinity of the interconnection. The activation energy in the interconnection was increased from 0.54 to 0.61 eV by improving the crystallinity due to the annealing at 400°C after electroplating. The estimated lifetime of the interconnection annealed at 400°C was about 20 times longer than that of as-electroplated interconnection. Therefore, the control of the crystallinity is indispensable for improving the reliability of electronic devices.  
**Keywords:** Gold bump, Interconnection, Electromigration, Crystallinity
Paper ID: 4066*
Multi-Channel Dumb-bell shaped Graphene Nanonibbon Structure to Elucidate Electronic Fluctuations for an Enhanced Performance
Jowesh Goundar, Takuya Kudo, Qinqiang Zhang, Ken Suzuki, Hideo Miura
Tohoku University, Japan
Abstract: Recent studies have indicated large fluctuations in graphene nanoribbon (GNR) based devices. Numerous reasons contribute to these fluctuations, however, a major reason is the formation of a reliable ohmic contact between the semi-conductive GNR, and the metallic electrodes. Here, we present a novel mechanism that elucidates the fluctuations by using multi-channel GNR's. A novel design based on a dumb-bell shaped graphene components, structured in an array proves to show a reliable performance of a GNR based device. The electronic performance and photoresponsivity was investigated by fabricating a GNR based field effect transistor (GNR-FET).
Keywords: Graphene, Dumb-bell Shaped GNR, Photosensitivity, Graphene nanoribbon field effect transistor

Paper ID: 4068*
Thermal stress tracking in multi-die 3D stacking structure by finite element analysis
Cheong-Ha Jung, Won Seo, Eunsol Jo, Gu-sung Kim
Kangnam University, Korea
Abstract: Ansys v.2019 R2 was used to analyze the thermal reliability problems of the 3D stacked package. As shown in Fig. 1, the 3D structure of multi die stacked with 4 layers was modeled and the thermal cycling test according to the JEDEC22 A104 standard was simulated. As a result, the maximum stress was generated at the solder joint of the TMV located at the lowest layer, and the minimum stress occurred at the untested EMC, where the thermal load was in direct contact with the deformation. Therefore, if the solder joint, which is considered as a weak point of TMV, is reinforced, the reliability of the package will be improved.
Keywords: 3D stacking, Finite Element Analysis, Thermal stress

Paper ID: 4069*
Hierarchical Design Methodology and Optimization for Proximity Communication based Contactless 3D ThruChip Interface
Srinivasan Gopal¹, Deukhyoun Heo², Tanay Karnik¹
¹Intel Corporation, United States; ²Washington State University, United States
Abstract: For the first time, this work systematically develops the complete serial link by using hierarchical modeling with serial link power and delay models. This paper presents a comprehensive design methodology and optimization using analytical expressions that analyzes the intrinsic energy and area trade-offs of an inductive coupling based high speed serial link. Further, we also demonstrate that equalization is a potential technique of breaking the intrinsic energy and area trade-offs of a TCI channel and reduces link power consumption and inductor area.
Keywords: TCI, Inductive Coupling, 3D IC, Proximity Communication

*Student Papers
PROGRAM SCHEDULE – October 9, 2019 (Miyagino Ward Cultural Center)

13:30-15:00  B4P-C, Poster Session Core Time at PatoNa Theater (Continued)

Paper ID: 4070  
Collective and Gang Bonding for Three-Dimensional Integrated Circuits in Chip-on-Wafer Process  
Hiroto Tanaka, Yoshiyuki Arai, Toshiyuki Jinda, Noboru Asahi, Katsumi Terada  
Toray Engineering Co., Ltd., Japan  
Abstract: We report on a thermal compression post-bonder (PB3000W) that can simultaneously bond 2–6 cubes and an eight-layer stacked integrated circuit on a wafer in a two-step bonding process. This bonder can perform both collective bonding and gang bonding. The throughput can be remarkably improved because multiple layers of chips can be pre-bonded using a pre-applied non-conductive film adhesive activated simultaneously for multiple chip layers with thermal pressure. Therefore, this bonder has a high throughput of over 7000 UPH. To perform both collective and gang bonding, this bonder is equipped with a new structure head for gang bonding, a backup stage with a pulse heater, and support stages as a heat sink and wafer holder.  
Keywords: Wafer bonding, Gang bonding, Collective bonding, Warpage, NCF

Paper ID: 4071  
Investigation of the Underfill with Negative-Thermal-Expansion Material to Suppress Mechanical Stress in 3D Integration System  
Hisashi Kino, Takafumi Fukushima, Tetsu Tanaka  
Tohoku University, Japan  
Abstract: Three-dimensional (3D) integration process is a promising method to enhance electronic device performance. Conventional 3D integration systems consist of vertically stacked several thin IC chips those are electrically connected with lots of through-Si vias (TSVs) and metal microbumps. Metal microbumps are surrounded by organic adhesive. An epoxy-based material, so-called underfill, has been widely used to fill the gap between several chips. In general, the coefficient of thermal expansion (CTE) of the underfill material is larger than that of metal microbumps. This CTE mismatch induces local bending stress in thinned IC chips. This local bending stress would affect the CMOS circuit in thinned IC chips. Therefore, we should suppress the local bending stress to realize 3D IC with high reliability. In this study, we propose a novel underfill with negative-thermal-expansion material which can suppress the local bending stress in 3D integration systems.  
Keywords: 3D integration, negative thermal expansion
PROGRAM SCHEDULE – October 9, 2019 (Miyagino Ward Cultural Center)

15:00-16:40  B5L-B, Session 4: Memory System
Session Co-Chairs: Prof. Takayuki Ohba, Tokyo Institute of Technology
Prof. Makoto Nagata, Kobe University

Paper ID: 4085
Presentation time: 15:00-15:30
Invited Talk: An Introduction to Marching Memory (MM)
Tadao Nakamura
Keio University, Japan

Abstract: Today’s computer systems rather have a big issue, which is what is called the memory bottleneck, especially as their scale has been growing with nanotechnology year by year toward EXA-scale supercomputing for scientific calculations and deep learning in neural-networking. To solve the issue, we must be back to the origin of computer system design pursuing what memory in computer systems should be. We are developing Marching Memory (MM), and can show how the features of it suit the solution with reasonable conditions such as higher speed with no latency under lower power consumption than SRAM.

Keywords: memory bottleneck, memory bottleneck, deep learning, serial data transfer, serial data transfer

Paper ID: 4081
Presentation time: 15:30-16:00
Invited Talk: Future Challenges to Packaging Technologies of High Bandwidth Memory
Ho-Young Son, Kangwook Lee
SK Hynix Inc., Korea

Abstract: High bandwidth memory (HBM) is a new and an innovative solution satisfying with semiconductor industry trends representing as the era of big data and cloud computing. SK hynix HBM1, world 1st DRAM product released in 2013 opened up the new era in memory industry by showing the excellent performance in a view of lower power and higher bandwidth and the possibility to expand the memory capacity by multi-die stacking with through silicon vias (TSVs). Starting from the high speed graphic applications, HBM is now expanding its possible applications to high performance computing, network server, accelerators and other SoC and it promotes a lot of packaging technology challenges to meet the needs of semiconductor industry market.

Keywords: HBM (High Bandwidth Memory), TSV (Through Silicon Via), KGSD (known-good-stacked-die), SiP (system-in-pacakge)
**High Bandwidth Memory (HBM) and High Bandwidth NAND (HBN) with the Bumpless TSV Technology**

**Koji Sakui**¹, **Takayuki Ohba**²

¹Honda Research Institute Japan Co., Ltd., Japan; ²Tokyo Institute of Technology, Japan

**Abstract:** This paper proposes a fundamental architecture for the High Bandwidth Memory (HBM) with the bumpless TSV for the Wafer-on-Wafer (WOW) technology. The bumpless interconnects technology can increase the number of TSVs per chip with fine pitch of TSVs, and reduce the impedance of the TSV interconnects with no bumps. Therefore, a further higher speed and higher density HBM can be realized. Also, the High Bandwidth NAND (HBN), which can read and program by plane instead of by line by using the bumpless TSV, has been proposed.

**Keywords:** wafer-on-wafer, bumpless, thinning, TSV, high density integration

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**Over-the-top Si Interposer Embedding Backside Buried Metal PDN to Reduce Power Supply Impedance of Large Scale Digital ICs**

**Takuji Miki**¹, **Makoto Nagata**¹, **Akihiro Tsukioka**¹, **Noriyuki Miura**¹, **Takaaki Okidono**², **Yuuki Araga**³, **Naoya Watanabe**³, **Haruo Shimamoto**³, **Katsuya Kikuchi**³

¹Kobe University, Japan; ²ECSEC, Japan; ³AIST, Japan

**Abstract:** A 2.5D structure with a Si interposer stacked on a CMOS chip is presented. A thick Cu backside buried metal (BBM) in Si Interposer provides low resistive power/ground wiring and also forms a large parasitic bypass capacitance between BBM and top metal, which suppresses the power supply noise. The Si interposer was implemented over an cryptographic chip with a large scale digital circuit fabricated in 130 nm CMOS. An internal noise monitoring circuit exhibits the proposed over-the-top Si interposer reduces a peak-to-peak power supply noise and DC drop during cryptographic operation to less than 50%.

**Keywords:** Interposer, 2.5D, TSV, PDN

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**16:40-16:55 Coffee Break/Exhibit Hours**
16:55-18:05  B6L-B, Session 5: Monolithic/Hetero Integration
Session Co-Chairs: Prof. Hisashi Kino, Tohoku University
Dr. Akihiro Noriki, AIST

Paper ID: 4077
Presentation time: 16:55-17:25
Invited Talk: Monolithic 3D as an Alternative to Advanced CMOS Scaling: Technology, Design and Architecture Perspectives
Pascal Vivet
CEA-LETI, France

Abstract: Monolithic 3D technology (M3D) is a promising alternative to tackle the loss of Moore's Law scaling beyond 22 nm node. By stacking different circuit layers thanks to nano-scale 3D Monolithic Inter Tier Via (MIV), it will be possible to offer a level of circuit integration never reached before, allowing advanced node scaling again as well as mixing heterogeneous technologies. M3D integrates sequentially different layers of transistors, with an ultra-fine pitch, in the 100 nm range, which is 200x smaller than state-of-the-art Through Silicon Vias (TSV) or 50x smaller than Copper to Copper Hybrid bonding (Cu-Cu HB). This high density 3D integration will pave the way towards new architectures, such as neuro- and bio-inspired applications, ultra-high density memory-computing cube and smarter mixed signal devices within tight low power constraints. This talk presents an overview of M3D technology and potential applications, and in more detail its associated design challenges, respectively on physical implementation aspects and on thermal dissipation.

Keywords: 3DIC, Monolithic 3D, CoolCubeTM, Physical Design tools, Thermal effect

Paper ID: 4047*
Presentation time: 17:25-17:45
Fabrication of high quality InAs-on-Insulator structures by Smart Cut process with reuse of InAs wafers
Kei Sumita, Jun Takeyasu, Kimihiko Kato, Kasidit Toprasertpong, Mitsuru Takenaka, Shinichi Takagi
The University of Tokyo, Japan

Abstract: InAs-On-Insulator structures are fabricated by the Smart Cut process and reusability of the donor InAs wafer without the degradation of film quality is also demonstrated. The effects of thermal annealing, which is expected to recover the damage induced by the implantation process, on the InAs-OI quality are studied. It is shown that annealing at 500 °C is effective to recover the crystallinity and as a result, 140-nm-thick (111) InAs-OI fabricated by the reusing process is shown to have the electron Hall mobility of 6500 cm2/Vs and the carrier density of 6 x 10^17 /cm3.

Keywords: Monolithic 3D, Direct wafer bonding, InAs-OI

*Student Papers
Vertical Optical and Electrical Interconnection for Chip-Scale-Packaged Si Photonic Transceivers

Koichi Takemura¹, Akio Ukita¹, Yasuhiro Ibusuki¹, Mitsuru Kurihara¹, Akihiro Noriki², Takeru Amano², Daisuke Okamoto¹, Yasuyuki Suzuki¹, Kazuhiko Kurata¹

¹PETRA, Japan; ²AIST, Japan;

Abstract: Chip-scale-packaged Si photonic optical transceiver modules with high density 3-dimensional optical and electrical I/O structures have been developed. The optical I/O is a vertical polymer waveguide structure made of UV curable resins. The waveguide structure includes 125-μm-pitch 8°-tilted cores formed by oblique-illuminated photolithography. The electrical I/O structure comprises 250-μm-pitch regularly arranged through-glass-vias. These I/O structures are placed on the same side of the Si photonic IC chip. This configuration enables simultaneous optical and electrical bonding to polymer-waveguide-embedded printed circuit boards. The developed I/O structures minimize area penalty and support 25 Gb/s multimode transmission.

Keywords: Silicon photonics, Optical interconnection, Optical pin, TGV, Polymer waveguide
08:45 Registration Starts

09:20-10:20 C1L-B
Special Session: IEEE ELECTRONICS PACKAGING AWARD 2020 Recipients Talk
Session Chair: Prof. Tetsu Tanaka, Tohoku University

Paper ID: 4088
Presentation time: 09:20-09:50
Past, present and future of 3DIC
Mitsumasa Koyanagi
Tohoku University, Japan

Abstract: Firstly I proposed to introduce a concept of 3D integration to DRAM and invented a 3D stacked capacitor DRAM cell in 1976 which has been widely used in the DRAM production. The stacked capacitor DRAM cell was the first commercialized 3D device. Various technologies and materials were integrated into the stacked capacitor DRAM cell which can be called a heterogeneous integration. This concept has been extended to a chip-level and wafer-level 3D integration using TSV in 1989. We succeeded in fabricating the first proto-type 3DICs with a block parallel architecture using TSV, 3D stacked image sensor in 1999, 3D memory in 2000, 3D artificial retina chip in 2001 and 3D microprocessor chip in 2002. These early works succeeded to Japan national projects of JST brain project (1997-2002), NEDO dream chip project (2008-2013) and JST dependable VLSI project (2009-2014) where 3D neuromorphic chips, 3D stacked image sensor with extremely high frame rate of 10,000 frames/s and 3D multicore processor with self-test and self-repair function were developed. We have proposed a new heterogeneous 3D integration technology based on a self-assembly called a super chip for future 3D systems. In addition, we have been developing a 3D reconfigurable AI chip with a new cyclic architecture for future edge application.

Paper ID: 4061
Presentation time: 09:50-10:20
Fraunhofer's Initial and Ongoing Contributions in 3D IC Integration
Peter Ramm1, Armin Klumpp1, Christof Landesberger1, Josef Weber1, Andy Heinig2, Peter Schneider2, Guenter Elst2, Manfred Engelhardt3
1Fraunhofer EMFT, Germany; 2Fraunhofer IIS-EAS, Germany; 3Senior Principal Emeritus Infineon, Germany

Abstract: Fraunhofer has been working on 3D integration since end of 1980’s, when they successfully fabricated 3D CMOS devices based on recrystallization of Poly-Si. Then, in a cooperative project with Siemens we were the first to demonstrate a complete industrial 3DIC stacking process (1993-1996) based on wafer bonding and vertical integration of IC devices using inter-chip vias (later called TSV). Starting 1999, we investigated 3D TSV technologies with particular focus on die-to-substrate stacking and initiated the European Integrating Projects e-CUBES®, and e-BRAINS, where we evaluated the application of 3D heterogeneous integration, including demonstration of high-performance communications. In this paper we will also present ongoing developments in heterogeneous integration and approaches for systematic hierarchical modelling in order to carry out simulations in different physical domains, based on a unified description of the 3D system.

Keywords: 3DIC, TSV, Wafer Bonding, Vertical Interconnections, Heterogeneous Integration
Invited Talk: Future Directions for 3DIC Technology and Design
Paul D. Franzon
North Carolina State University, United States

Abstract: 3DICs have had major impact on memories and image sensors. What is next?
First, we will make the case for memories with performance and power efficiency levels well beyond those of today. These will be largely driven by machine learning and artificial intelligence workloads. While the needs of convolutional neural networks can be met by HBM, other algorithms such as Multi-layer perceptron (MLP) and Long Short Term Memory require a lot more memory accesses per operation. Emerging cortically inspired algorithms, such as Hierarchical Temporal Memory, require even more bandwidth. We will describe some samples of what new memory architectures might look like and how their cost and performance are related to the underlying TSV technology.
Despite considerable research there have been little commercial takeup of logic on logic 3D chip stacks. This is despite the potential for logic on logic to help in scaling beyond that achieved by Moore’s Law alone. This potential will be realized as we approach the 5 nm node and hybrid bonding technology achieves its full potential. The case for 3D logic will be made based on a combination of technology push and cost-performance scaling pull.
Chiplets integrated using interposers also have considerable potential for resulting in widespread 3D adoption. Results of recent experiments designing chiplets for machine learning will be presented along with anticipated results.

Design enablement of fine pitch face-to-face 3D system integration using die-by-die place & route
Giuliano Sisto1,2,3, Peter Debacker2, Rongmei Chen2, Geert Van der Plas2, Richard Chou1, Eric Beyne2, Dragomir Milojevic2,3
1Cadence Design Systems, United States; 2imec, Belgium; BEAMS, 3Ecole Polytechnique de Bruxelles, Belgium

Abstract: In this paper we are presenting an innovative design methodology for Face-to-face Hybrid bonded 3D IC, leveraging on a 3D aware placement of cells and macros. The complete flow is described, starting from synthesis, with the definition of a 3D netlist, ending up with signoff measurements. In fact, in terms of experimental results, a comparison with the same design, built in a standard 2D fashion, is provided. Timing and wirelength have been used as main metrics for this comparison. This work is the result of a close collaboration between Cadence Design Systems and IMEC.

Keywords: Die Stacking, Hybrid Bonding, Face-to-face, 3D IC, Sequential 3D

*Student Papers
**Program Schedule – October 10, 2019 (Miyagino Ward Cultural Center)**

10:35-12:05  C2L-B, Session 6: 3D Design (Continued)

**Paper ID: 4037**  
**Presentation time: 11:25-11:45**  
**An Accurate Assessment of Chip-Package Interaction Is a Key Factor for Designing Resilient 3D IC Systems**  
Valeriy Sukharev, Armen Kteyan, Jun-Ho Choy  
*Mentor, a Siemens Business, Armenia; Mentor, a Siemens Business, United States*  
**Abstract:** Recently developed a novel physics-based model and a multiphysics EDA tool-prototype provide for the first time a capability for analyzing temperature, stress and deformation fields with a feature-scale resolution everywhere across a chip (dies & package), which were generated immediately upon chip assembly and during chip operation. This kind of assessment allows to avoid many reliability problems such, for example, as a possible stack de-bonding and to address an interference of the CPI-induced stresses with the stresses carefully engineered in transistor channels, which can destroy the on-currents of transistors and affect the chip performance.  
**Keywords:** 3D IC, CPI, reliability, temperature, stress

**Paper ID: 4063**  
**Presentation time: 11:45-12:05**  
**Merging PDKs to build a design environment for 3D circuits: methodology, challenges and limitations**  
Olivier Billoint, Karim Azizi-Mourier, Gérald Cibrario, Didier Lattard, Mehdi Mouhdach, Sébastien Thuries, Pascal Vivet  
*CEA, LETI, France*  
**Abstract:** Design of 3D ICs is mainly done in separated design environments for each tier, assuming that communication channels between tiers are user-defined and fixed at the beginning of the design process. Suitable for 3D stacking based on TSV or Hybrid Bonding technologies because of the low granularity of these 3D interconnect elements, this methodology becomes more difficult to apply to 3D sequential technologies once trying to integrate Monolithic Inter-tier Vias (MIV) with higher density (around 1.108 vias per mm2). In this paper, we describe a methodology to create a unified design environment, which includes several technologies attached to different tiers.  
**Keywords:** PDK, Design environment, Addon

12:05-13:30  Lunch Time/Exhibition Hours

*Student Papers*
13:30-15:00  C3L-B, Session 7: Direct/Hybrid Bonding
Session Co-Chairs: Dr. Fumihiro Inoue, imec
Prof. Sarah Kim, Seoul National University of Science and Technology

Paper ID: 4084
Presentation time: 13:30-14:00
Invited Talk: Innovative Bonding Technology for 3D Integration
Tadatomo Suga
Meisei University, Japan
Abstract: Effectiveness of the surface activation for room temperature bonding was demonstrated in the middle of '80, for example, for Al-Al and Al-Si3N4 in 1992, for Cu-Cu micro-bonding in 1993, and for the direct wafer bonding of Si-Si in 1996. The method is called as the surface activated bonding (SAB) and has been developed for heterogeneous bonding between different materials at room temperature, attracting increasing interest due to its simple process flow, no need for additional intermediate materials for bonding, and compatibility with CMOS technology. The standard SAB method is based on surface bombardment by Ar beam in ultra-high vacuum to clean the surfaces so that they can be bonded very strongly at room temperature without heat treatment. Modifications of the surface activation have been investigated to extend the standard SAB method for various materials and applications. The standard SAB method uses Ar beam bombardment to remove surface adsorption and oxidation layer to realize bonding between semiconductors when two surfaces are brought into contact. It has been studied for bonding of Si-Si, Ge-Ge, and compound semiconductors such as GaAs-Si.
Keywords: Low temperature bonding, room temperature bonding, heterointegration surface activated bonding, wafer bonding

Paper ID: 4050
Presentation time: 14:00-14:20
A 6.9 μm Pixel-Pitch 3D Stacked Global Shutter CMOS Image Sensor with 3M Cu-Cu connections
Tsukasa Miura, Masaki Sakakibara, Hirotugu Takahashi, Tadayuki Taura, Keiji Tatani, Yusuke Oike, Takayuki Ezaki
Sony Semiconductor Solutions, Japan
Abstract: In this paper, we report on a 3D stacked global shutter CMOS image sensor with 3M Cu-Cu connections. Using a fine pitch and a large amount of Cu-Cu connection technology, we achieved 1.46M pixels of 6.9 μm × 6.9 μm size. The pixel evaluation result shows that all 3M Cu-Cu connections have been successfully conducted.
Keywords: Cu-Cu, bonding, 3D stacked, CMOS, image sensor, ADC

*Student Papers
PROGRAM SCHEDULE – October 10, 2019 (Miyagino Ward Cultural Center)

13:30-15:00  C3L-B, Session 7: Direct/Hybrid Bonding (Continued)

Paper ID: 4019
Presentation time: 14:20-14:40
Die-to-Wafer Direct Hybrid Bonding Demonstration with High Alignment Accuracy and Electrical Yields
Amandine Jouve¹, Loïc Sanchez¹, Clément Castan¹, Nicolas Bresson¹, Frank Fournel¹, Severine Cheramy¹, Nicolas Raynaud², Pascal Metzger²
¹CEA, LETI, France; ²SET, France
Abstract: Die-To-Wafer (D2W) direct hybrid bonding is foreseen as a major breakthrough for the future of 3D components; however, its industrialization rises some additional challenges compared to Wafer-To-Wafer processing. This paper presents a 300mm wafer complete solution developed at LETI to improve bonding yield of D2W hybrid bonding using copper interconnections until the assessment of the electrical performances thanks to a dedicated 300mm electrical test vehicle and robust stacking system. Stackings with +/-1.5µm accuracy and excellent bonding interface have been obtained (80% bonding yield). After stacking and annealing, the die can be thinned down to 10µm without damage. Electrical yield measured on daisy-chains with more than 20,000 connections present more than 75% yield and shown very limited drift after preliminary environmental reliability tests. All these results confirmed the high industrial potential of D2W hybrid bonding technology.
Keywords: 3D, Direct Hybrid Bonding, Die-To-Wafer, Contact resistance

Paper ID: 4020
Presentation time: 14:40-15:00
Toward a Complete Direct Hybrid Bonding D2W Integration flow: Known-good-Dies and Die planarization Modules Development
Emilie Bourjot, Paul Stewart, Christophe Dubarry, Emmanuelle Lagoutte, Emmanuel Rolland, Nicolas Bresson, Amandine Jouve, Daniel Scevola, Viorel Balan
CEA-Leti, France
Abstract: Die-to-wafer stacking is very promising for the next 3DIC generation since it offers the ability to assemble several dies with small interconnection pitches. This paper proposes an overall integration scheme D2W HB process to reinforce its robustness and its economical relevance for microelectronics industry. Firstly, a KGD strategy was developed to be compatible with hybrid bonding. A successful D2W bonding was demonstrated with tested pads. Secondly, the development of the planarization of stacked dies is presented.
Keywords: D2W, direct hybrid bonding, KGD, known good dies, planarization

15:00-15:15  Coffee Break
PROGRAM SCHEDULE – October 10, 2019 (Miyagino Ward Cultural Center)

15:15-16:25, C4L-B, Session 8: Thermal Management
Session Chair: Dr. Shinichi Ogawa, AIST
    Prof. Takafumi Fukushima, Tohoku University

Paper ID: 4082
Presentation time: 15:15-15:45
Invited Talk: Heat Transfer in Nanostructured Si and Heat Flux Control Technique
Masahiro Nomura
The University of Tokyo, Japan
Abstract: Heat transfer in Si nanostructure is not only an interesting topic in fundamental physics, but also an important practical study for efficient heat dissipation in electronic devices. In this talk, fundamentals of thermal phonon transport in nanostructured Si will be explained and some technique to control heat flux in Si membrane by nanostructuring will be introduced.
Keywords: Phonon, heat transfer, phonon engineering, phononic crystal

Paper ID: 4033
Presentation time: 15:45-16:05
Vertical Stack Thermal Characterization of Heterogeneous Integration and Packages
Robert Harris¹, Rhett Davis², Steve Lipa², Shepherd Pitts², Paul Franzon²
¹GTRI, United States; ²NCSU, United States
Abstract: This paper presents thermal measurement data of GaN HEMT on CMOS HI using a Diverse Accessible Heterogeneous Integration (DAHI) process. Thermal T3ster measurements, a product and service available from Mentor are presented. The method uses thermal transients to characterize the vertical thermal path stack including the package. Here the thermal dominance of the thermal interface at the die attachment is apparent. The T3ster measurements are contrasted with in-channel micro-Raman thermal measurements along with simulated results.
Keywords: thermal, Heterogeneous, gan, 2.5d, simulation, measurement

*Student Papers
PROGRAM SCHEDULE – October 10, 2019 (Miyagino Ward Cultural Center)

15:15-16:25, C4L-B, Session 8: Thermal Management (Continued)

Paper ID: 4042
Presentation time: 16:05-16:25
Thermal Stress Comparison of Annular-Trench-Isolated (ATI) TSV with Cu and Solder Core
Wei Feng, Naoya Watanabe, Haruo Shimamoto, Masahiro Aoyagi, Katsuya Kikuchi
National Institute of Advanced Industrial Science and Technology, Japan

Abstract: In order to reduce the thermal stress in Si substrate, we proposed a novel Through Silicon Via (TSV) structure as annular-trench-isolated (ATI) TSV. Considering the origin of thermal stress, the material of TSV affects thermal behavior. In this paper, we compared the thermal stress of ATI TSV with Cu and Solder core materials. A numerical model of ATI TSV was established to simulate and analyze the thermal stress with different metal core materials by varying the temperature from 25°C to 125°C and -55°C. The simulation results showed a similar stress distribution for two core materials. And the thermal stress variation profiles near the device area were also analyzed. Although the ATI TSV with Solder core showed lower stress in the core area, the stress outside Si ring is at the same level for two core materials.

Keywords: TSV, thermal stress, FEM simulation

16:25-17:00  Student Award Ceremony & Closing Ceremony

*Student Papers
ACCESS TO DAY 2 & 3 CONFERENCE VENUE

MIYAGINO WARD CULTURAL CENTER

Access to Miyagino Ward Cultural Center in Sendai from Sendai Station (3DIC 2019 Conference Venue for October 9 and 10)
Please be noted that the first day of the conference, October 8, is Hotel Metropolitan Sendai which is 1-minute walking distance from Sendai Station.

仙台駅から宮城野区文化センター(10/9, 10/10の会場)へのアクセス

Take JR Senseki Line to Rikuzen Haranomachi Station (3rd stop, 6-minute ride)
The Miyagino Ward Cultural Center is located in front of the station.
JR 仙台駅から仙石線下り方面行きで3つ目、6分、陸前原ノ町駅下車すぐ

Take Track 10 bound for Matsushima Kaigan, Ishinomaki and get off at Rikuzen Haranomachi Station, 3rd stop from Sendai.

The conference venue, Miyagino Ward Cultural Center is located in front of the Rikuzen Haranomachi Station.