3DIC 2019 Program Schedule
October 8-10, 2019 **as of September 8, 2019**
Conference Venue:
October 8, 2019 at Hotel Metroloplitan Sendai
October 9-10, 2019 at Miyagino Ward Cultural Center in Sendai

Session Date	Session	Session time	Presentation time	paper_id	Category	paper_title	Authors	Affiliations
08-Oct-19	Plenary Talk I	13:30-14:10	13:30-14:10	4073	Plenary	On why dielets are the new craze for heterogeneous Integration	Subramanian S. Iyer	University of California, Los Angeles, United States
08-Oct-19	Session 1: 3D Stacked Imager	14:10-16:05	14:10-14:40	4078	Invited	3D Integration Technologies for Stacked CMOS Image Sensors	Yoshihisa Kagawa, Hayato Iwamoto	Sony Semiconductor Solutions Corporation, Japan
08-Oct-19	Session 1: 3D Stacked Imager	14:10-16:05	14:55-15:25	4083	Invited	Universal ADC for Sensor Applications	Akira Matsuzawa	Tech Idea Co., Ltd., Japan
08-Oct-19	Session 1: 3D Stacked Imager	14:10-16:05	15:25-15:45	4018	Lecture	Triple-Layering Technology for Pixel-Parallel CMOS Image Sensors Developed by Hybrid Bonding of SOI Wafers	Masahide Goto{2}, Yuki Honda{2}, Toshihisa Watabe{2}, Kei Hagiwara{2}, Masakazu Nanba{2}, Yoshinori Iguchi{2}, Takuya Saraya{3}, Masaharu Kobayashi{3}, Eiji Higurashi{1}	{1}National Institute of Advanced Industrial Science and Technology, Japan; {2}NHK Science and Technology Research Laboratories, Japan; {3}The University of Tokyo, Japan
08-Oct-19	Session 1: 3D Stacked Imager	14:10-16:05	15:45-16:05	4046	Lecture	3D Integrated Pixel Sensor with Silicon-on-Insulator Technology for the International Linear Collider Experiment	Miho Yamada{3}, Shun Ono{1}, Yasuo Arai{1}, Toru Tsuboyama{1}, Makoto Motoyoshi{2}	{1}High Energy Accelerator Research organization (KEK), Japan; {2}Tohoku-MicroTec Co., Ltd.,, Japan; {3}Tokyo Metropolitan College of Industrial Technology, Japan
08-Oct-19	Session 2: Integration Technology I	16:20-17:50	16:20-16:50	4080	Invited	Power-Performance Advantages of InFO Technology in System Integration	Chuei-Tang Wang	Taiwan Semiconductor Manufacturing Company Limited, Taiwan
08-Oct-19	Session 2: Integration Technology I	16:20-17:50	16:50-17:10	4012	Lecture	Investigation of Low Temperature Cu Pillar Eutectic Bonding for 3D Chip Stacking Technology	Yi-Chieh Tsai, Chia-Hsuan Lee, Kuan-Neng Chen	National Chiao Tung University, Taiwan
08-Oct-19	Session 2: Integration Technology I	16:20-17:50	17:10-17:30	4016	Lecture	Process Complexity and Cost Considerations of Multi-Layer Die Stacks	Dimitrios Velenis, Joeri De Vos, Soon-Wook Kim, Jaber Derakhshandeh, Pieter Bex, Giovanni Capuz, Samuel Suhard, Kenneth June Rebibis, Stefaan Van Huylenbroeck	imec, Belgium
08-Oct-19	Session 2: Integration Technology I	16:20-17:50	17:30-17:50	4041	Lecture	A Graph-Based Model of Micro-Transfer Printing for Cost-Optimized Heterogeneous 2.5D Systems	Robert Fischbach, Tilman Horst, Jens Lienig	Dresden University of Technology, Germany
09-Oct-19	Plenary Talk II	09:00-09:40	09:00-09:40		Plenary	TBA	TBA	TBA
09-Oct-19	Plenary Talk III	09:40-10:20	09:40-10:20	4075	Plenary	Quantum annealing and its application - new generation of natural computing	Masayuki Ohzeki	Tohoku University, Japan
09-Oct-19	Session 3: Integration Technology II	10:35-12:05	10:35-11:05	4079	Invited	Advances in Substrate Manufacturing for AI/HPC and 5G Packaging	Farhang Yazdani	BroadPak Corporation, United States
09-Oct-19	Session 3: Integration Technology II	10:35-12:05	11:05-11:25	4049	Lecture	High density low-temperature interconnection enabled by mechanical self-alignment and electroless plating	Sreejith Kochupurackal Rajan{1}, Ming Jui Li{1}, Gary May{2}, Muhannad Bakir{1}	{1}Georgia Institute of Technology, United States; {2}University of California, Davis, United States
09-Oct-19	Session 3: Integration Technology II	10:35-12:05	11:25-11:45	4013	Lecture	Design Considerations and Fabrication Challenges of Surface Electrode Ion Trap with TSV Integration	Jing Tao{2}, Hong Yu Li{1}, Peng Zhao{2}, Yu Dian Lim{2}, Anak Agung Alit Apriyana{2}, Chuan Seng Tan{2}	{1}Institute of Microelectronics, Singapore; {2}Nanyang Technological University, Singapore
09-Oct-19	Session 3: Integration Technology II	10:35-12:05	11:45-12:05	4011	Lecture	Fabrication and Morphology Analyses of Nano-Scale Interconnects for 3D-Integaration	Murugsan Mariappan, Takafumi Fukushima, Hiroyuki Hashimoto, Jichel Bea, Mitsumasa Koyanagi	Tohoku University, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4002	Poster	Misalignment Analysis and Electrical Performance of High Density 3D-IC Interconnects	Imed Jani, Didier Lattard, Pascal Vivet, Lucile Arnaud, Edith Beignｦｸ	CEA-LETI, France
09-Oct-19	Poster Session Core time*	13:30-15:00		4003	Poster	Effects of Argon and Nitrogen Ion Bombardments on Sputtered and Electroplated Cu Surfaces for Cu Bonding Application	Sarah Kim, Han Kyeol Seo, Hae-Sung Park	Seoul National University of Science and Technology, Korea
09-Oct-19	Poster Session Core time*	13:30-15:00		4004	Poster	Characterization of Nitride Passivated Cu Surface for Low-Temperature Cu-Cu Bonding	Sarah Kim, Hae-Sung Park, Han Kyeol Seo	Seoul National University of Science and Technology, Korea
09-Oct-19	Poster Session Core time*	13:30-15:00		4006	Poster	Tin Guard Ring Around TSV for Cross-Talk Suppression of Parallel Networking Lines of Data Center	Alit Apriyana Anak Agung, Chuan Seng Tan	NTU, Singapore
09-Oct-19	Poster Session Core time*	13:30-15:00		4007	Poster	Low-Temperature Wafer-Level Au-Au Bonding at 100 ℃	Po-Chih Chen, Demin Liu, Kuan-Neng Chen	National Chiao Tung University, China; National Chiao Tung University, Taiwan
09-Oct-19	Poster Session Core time*	13:30-15:00		4008	Poster	Low Temperature Cu-Cu Direct Bonding Below 150°C with Au Passivation Layer	Demin Liu, Po-Chih Chen, Yi-Chieh Tsai, Kuan-Neng Chen	National Chiao Tung University, China; National Chiao Tung University, Taiwan
09-Oct-19	Poster Session Core time*	13:30-15:00		4009	Poster	Temperature Cycling Reliability of Wow Bumpless Through Silicon Vias	Chia-Hsuan Lee{2}, Hsin-Chi Chang{1}, Jui-Han Liu{1}, Hiroyuki Ito{2}, Young Suk Kim{2}, Kuan-Neng Chen{1}, Takayuki Ohba{2}	{1}Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan, Taiwan; {2}First, Tokyo Institute of Technology, Tokyo, Japan, Japan

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09-Oct-19	Poster Session Core time*	13:30-15:00		4014	Poster	Noise Performance Improvement in Future IC Integration Using Perylene-N As Dielectric Material	Pragathi Dadaipally, N. Arun Vignesh, Ch. Usha Kumari, Sudharsan Jayabalan, T. Santosh Kumar, Tatiparti Padma, Asisa Kumar Panigrahy	Gokaraju Rangaraju Institute of Engineering & Technology, Hyderabad, India
09-Oct-19	Poster Session Core time*	13:30-15:00		4015	Poster	Protective Layer for Collective Die to Wafer Hybrid Bonding	Fumihiro Inoue{1}, Julien Bertheau{1}, Samuel Suhard{1}, Alain Phommahaxay{1}, Takuya Ohashi{2}, Tetsuro Kinoshita{2}, Yohei Kinoshita{2}, Eric Beyne{1}	{1}imec, Belgium; {2}TOK, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4017	Poster	Multichip CMOS Image Sensor Structure for Flash Image Acquisition	Yoshiaki Hagiwara	AIPS, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4021	Poster	Variability Cancellation to Improve Diagnostic Performance of Testing Through Silicon Vias in Power Distribution Network of 3D-IC	Koutaro Hachiya{2}, Atsushi Kurokawa{1}	{1}Hirosaki University, Japan; {2}Teikyo Heisei University, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4022	Poster	Electrical Field Test Method of Resistive Open Defects Between Dies by Quiescent Currents Through Embedded Diodes	Masaki Hashizume{2}, Hanna Soneda{2}, Hiroyuki Yotsuyanagi{2}, Shyue-Kung Lu{1}	{1}National Taiwan University of Science and Technology, Taiwan; {2}Tokushima University, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4023	Poster	On Delay Elements in Boundary Scan Cells for Delay Testing of 3D IC Interconnection	Toshiaki Satoh, Hiroyuki Yotsuyanagi, Masaki Hashizume	Tokushima University, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4024	Poster	Growth Optimization of Multi-Layer Graphene for Thermal-TSV Application in 3D-LSI	Murugesan Mariappan, Takafumi Fukushima, Mitsumasa Koyanagi	Tohoku University, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4025	Poster	Characterization of Low-Height Solder Microbump Bonding for Fine-Pitch Inter-Chip Connection in 3DICs	Yuki Miwa, Sungho Lee, Rui Liang, Kousei Kumahara, Hisashi Kino, Takafumi Fukushima, Tetsu Tanaka	Tohoku University, China; Tohoku University, Korea; Tohoku University, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4026	Poster	Development of Laser-Assisted Bonding with Compression (LABC) Process for 3D IC Integration	Kwang-Seong Choi{1}, Yong-Sung Eom{1}, Seok Hwan Moon{1}, Jiho Joo{1}, Kwangjoo Lee{2}, Jung Hak Kim{2}, Ju Hyeon Kim{2}	{1}ETRI, Korea; {2}LG Chem, Korea
09-Oct-19	Poster Session Core time*	13:30-15:00		4028	Poster	A Built-in Self-Test Scheme for TSVs of Logic-DRAM Stacked 3D ICs	Wei-Hsuan Yang{3}, Jin-Fu Li{3}, Chun-Lung Hsu{2}, Chi-Tien Sun{2}, Shih-Hsu Huang{1}	{1}Chung Yuan Christian University, Taiwan; {2}ITRI, Taiwan; {3}National Central University, Taiwan
09-Oct-19	Poster Session Core time*	13:30-15:00		4029	Poster	Cu Diffusion Barrier Properties of Various CoWB Electroless Plated Films	Taro Matsudaira{2}, Shunsuke Shindo{2}, Kosei Morita{2}, Tomohiro Shimizu{2}, Takeshi Itoh{2}, Shoso Shingubara{2}, Satoru Shimizu{1}	{1}JCU Corporation, Japan; {2}Kansai univ., Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4030	Poster	Photoresist Development for wafer-Level Packaging Process	Makiko Irie	Tokyo Ohka Kogyo Co., LTD, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4031	Poster	SiN used as a stressor in Germanium-On-Insulator substrate	Sethavut Duangchan{2}, Keisuke Yamamoto{4}, Dong Wang{4}, Hiroshi Nakashima{3}, Akiyoshi Baba{1}	{1}Center for Microelectronic Systems, Kyushu Institute of Technology, Japan; {2}Department of Industrial Physics and Medical Instrumentation, King Mongkut's University of Technolog, Thailand; {3}Global Innovation Center, Kyushu University, Japan; {4}Interdisciplinary Graduate School of Engineering Sciences, Kyushu University, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4032	Poster	Microstructural and Light Exposure Effects on Direct Copper to Copper Bonding	Zong-Yu Xie{2}, Jenn-Ming Song{2}, David Tarng{1}, Chih-Pin Hung{1}	{1}Advanced Semiconductor Engineering Group, Taiwan; {2}National Chung Hsing University, Taiwan
09-Oct-19	Poster Session Core time*	13:30-15:00		4034	Poster	Electrostatic Shield TSVs to Suppress Coupling Among Stacked ICs	Yuuki Araga, Katsuya Kikuchi, Masahiro Aoyagi	National Institute of Advanced Industrial Science and Technology (AIST), Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4035	Poster	Development of a CDS Circuit for 3-D Stacked Neural Network Chip Using CMOS Analog Signal Processing	Koji Kiyoyama{1}, Hiroyuki Hashimoto{2}, Hisashi Kino{2}, Takafumi Fukushima{2}, Tetsu Tanaka{2}, Mitsumasa Koyanagi{2}	{1}Nagasaki Institute of Applied Science, Japan; {2}Tohoku University, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4036	Poster	Study of macEtch Using Additives for Preparation of tsv	Shunsuke Hanatani, Takuya Yorioka, Tomohiro Shimizu, Takeshi Ito, Shoso Shingubara	kansai University, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4038	Poster	Low TCE Copper with annealing	Kazuo Kondo	Fine Feature Electrodeposition Research Laboratory, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4040	Poster	3D Test Wrapper Chain Optimization with I/O Cells Binding Considered	Fan-Hsuan Tang{1}, Hsu-Yu Kao{1}, Shih-Hsu Huang{1}, Jin-Fu Li{2}	{1}Chung Yuan Christian University, Taiwan; {2}National Central University, Taiwan

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09-Oct-19	Poster Session Core time*	13:30-15:00		4043	Poster	Cu-Cu Bonding Challenges with i-ACF® for Advanced 3D Integration	Shunji Kurooka{1}, Yoshinori Hotta{1}, Ai Nakamura{2}, Mitsumasa Koyanagi{2}, Takafumi Fukushima{2}	{1}FUJIFILM Corporation, Japan; {2}GINTI, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4044	Poster	Study of Optimizing Stress-Strain Curve of Adhesive for High Expansion Tape	Tadatomo Yamada, Ken Takano, Toshiaki Menjo, Shinya Takyu	LINTEC Corporation, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4045	Poster	Design of a 16kb SRAM in 3D Monolithic CoolCube technology	Adam Makosiej{1}, Pablo Royer{2}, Francois Andrieu{1}, Sebastien Thuries{1}, Pascal Vivet{1}, Edith Beigne{1}	{1}CEA-LETI, Minatec Campus, Univ. Grenoble Alpes, France; {2}STMicroelectronics, France
09-Oct-19	Poster Session Core time*	13:30-15:00		4048	Poster	Development of 3D-IC Embedded Flexible Hybrid System	Sungho Lee, Yuki Susumago, Zhengyang Qian, Noriyuki Takahashi, Hisashi Kino, Tetsu Tanaka, Takafumi Fukushima	Tohoku University, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4052	Poster	Optical TSV Using Si-Photonics Integrated Curved Micro-Mirror	Akihiro Noriki{1}, Isao Tamai{2}, Yasuhiro Ibusuki{2}, Akio Ukita{2}, Satoshi Suda{1}, Daisuke Shimura{2}, Yosuke Onawa{2}, Hiroki Yaegashi{2}, Takeru Amano{1}	{1}National Institute of Advanced Industrial Science and Technology, Japan; {2}Photonics Electronics Technology Research Association, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4053	Poster	A Design Scheme for 3-D Stacked CNN Accelerators	Jubee Tada{2}, Kazuto Takahashi{2}, Ryusuke Egawa{1}	{1}Tohoku University, Japan; {2}Yamagata University, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4054	Poster	X-ray photon-counting Imager with CdTe/Si-LSI stacking	Toru Aoki{2}, Katsuyuki Takagi{1}, Toshiyuki Takagi{2}, Hiroki Kase{2}, Akifumi Koike{1}	{1}ANSeeN Inc, Japan; {2}Shizuoka University, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4055	Poster	Transformer less floating gate driver for 3D power SoC	Minami Nakayama{1}, Seiya Abe{2}, Satoshi Matsumoto{2}	{1}Graduate School of Kyushu Institute of Technology, Japan; {2}Kyushu Institute of Technology, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4056	Poster	Investigation of the Influence of Material Properties on Warpage and Solder Joint Reliability of 2.5D & FO Package	Koji Hamaguchi, Kota Segawa, Mitsuki Nakata, Hitoshi Onozeki, Naoya Suzuki	Hitachi Chemical Co., Ltd, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4057	Poster	Design and Evaluation of a Novel and Ultra-compact Fully-TGV-based Self-shielding Bandpass Filter for 5G Applications	Ziyue Zhang{1}, Yingtao Ding{1}, Zhiming Chen{1}, Mingrui Zhou{1}, Miao Xiong{1}, Ziru Cai{1}, Xiao Gong{2}	{1}Beijing Institute of Technology, China; {2}National University of Singapore, Singapore
09-Oct-19	Poster Session Core time*	13:30-15:00		4058	Poster	Impacts of Deposition Temperature and Annealing Condition on Ozone-Ethylene Radical Generation-TEOS-CVD SiO2 for Low-Temperature TSV Liner Formation	Rui Liang, Sungho Lee, Yuki Miwa, Kousei Kumahara, Mariappan Murugesan, Hisashi Kino, Takafumi Fukushima, Tetsu Tanaka	Tohoku Univeristy, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4059	Poster	Hydrolysis-Tolerant Hybrid Bonding in Ambient Atmosphere for 3D Integration	Akitsu Shigetou{1}, Tilo Hongwei Yang{2}, Robert Kao{2}	{1}National Institute for Materials Science, Japan; {2}National Taiwan University, Taiwan
09-Oct-19	Poster Session Core time*	13:30-15:00		4062	Poster	Stacked Pixel Sensor / Detector technology using Au micro-bump Junction	Makoto Motoyoshi, Koki Yanagimura, Taiko Fushimi, Shunta Endo, Motoki Kobayashi, Hideaki Tamate	Tohoku-MicroTec Co., Ltd, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4064	Poster	Photoelectroscopic Study of Mn Barrier Layer on SiO2 for Si Wafer Bonding Process	Takahiro Nagata{1}, Kazumichi Tsumura{2}, Kenro Nakamura{2}, Kengo Uchida{2}, Jin Kawakita{1}, Toyohiro Chikyow{1}, Kazuyuki Higashi{2}	{1}National Institute for Materials Science, Japan; {2}Toshiba corporation, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4065	Poster	Crystallinity Dependence of Long-Term Reliability of Electroplated Gold Thin-Film Interconnections	Ken Suzuki, Ryota Mizuno, Yutaro Nakoshi, Hideo Miura	Tohoku University, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4066	Poster	Multi-Channel Dumb-bell shaped Graphene Nanonribbon Structure to Elucidate Electronic Fluctuations for an Enhanced Performance	Jowesh Goundar, Takuya Kudo, Qinqiang Zhang, Ken Suzuki, Hideo Miura	Tohoku University, Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4068	Poster	Thermal stress tracking in multi-die 3D stacking structure by finite element analysis	Won Seo, Eunsol Jo, Gu-sung Kim	Kangnam university, Korea
09-Oct-19	Poster Session Core time*	13:30-15:00		4069	Poster	Hierarchical Design Methodology and Optimization for Proximity Communication based Contactless 3D ThruChip Interface	Srinivasan Gopal{1}, Deukhyoun Heo{2}, Tanay Karnik{1}	{1}Intel Corporation, United States; {2}Washington State University, United States
09-Oct-19	Poster Session Core time*	13:30-15:00		4070	Poster	Collective and gang bonding for 3D-IC in CoW	Hiroto Tanaka, Yoshiyuki Arai, Toshiyuki Jinda, Noboru Asahi	Toray Engineering Co., Ltd., Japan
09-Oct-19	Poster Session Core time*	13:30-15:00		4071	Poster	Investigation of the Underfill with Negative-Thermal-Expansion Material to Suppress Mechanical Stress in 3D Integration System	Hisashi Kino, Takafumi Fukushima, Tetsu Tanaka	Tohoku University, Japan

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09-Oct-19	Session 4: Memory System	15:00-16:40	15:00-15:30	4085	Invited	An Introduction to Marching Memory (MM)	Tadao Nakamura	Keio University, Japan
09-Oct-19	Session 4: Memory System	15:00-16:40	15:30-16:00	4081	Invited	Future Challenges to Packaging Technologies of High Bandwidth Memory	Ho-Young Son, Kangwook Lee	SK Hynix Inc., Korea
09-Oct-19	Session 4: Memory System	15:00-16:40	16:00-16:20	4005	Lecture	High Bandwidth Memory (HBM) and High Bandwidth NAND (HBN) with the Bumpless TSV Technology	Koji Sakui{1}, Takayuki Ohba{2}	{1}Honda Research Institute Japan Co., Ltd., Japan; {2}Tokyo Institute of Technology, Japan
09-Oct-19	Session 4: Memory System	15:00-16:40	16:20-16:40	4051	Lecture	Over-the-top Si Interposer Embedding Backside Buried Metal PDN to Reduce Power Supply Impedance of Large Scale Digital ICs	Takuji Miki{3}, Makoto Nagata{3}, Akihiro Tsukioka{3}, Noriyuki Miura{3}, Takaaki Okidono{2}, Yuuki Araga{1}, Naoya Watanabe{1}, Haruo Shimamoto{1}, Katsuya Kikuchi{1}	{1}AIST, Japan; {2}ECSEC, Japan; {3}Kobe University, Japan
09-Oct-19	Session 5: Monolithic/Hetero Integration	16:55-18:05	16:55-17:25	4077	Invited	Monolithic 3D as an alternative to advanced CMOS scaling: technology, design and architecture perspectives	Pascal Vivet	CEA-Leti, France
09-Oct-19	Session 5: Monolithic/Hetero Integration	16:55-18:05	17:25-17:45	4047	Lecture	Fabrication of high quality InAs-on-Insulator structures by Smart Cut process with reuse of InAs wafers	Kei Sumita, Jun Takeyasu, Kimihiko Kato, Kasidit Toprasertpong, Mitsuru Takenaka, Shinichi Takagi	The University of Tokyo, Japan
09-Oct-19	Session 5: Monolithic/Hetero Integration	16:55-18:05	17:45-18:05	4060	Lecture	Vertical Optical and Electrical Interconnection for Chip-Scale-Packaged Si Photonic Transceivers	Koichi Takemura{2}, Akio Ukita{2}, Yasuhiro Ibusuki{2}, Mitsuru Kurihara{2}, Akihiro Noriki{1}, Takeru Amano{1}, Daisuke Okamoto{2}, Yasuyuki Suzuki{2}, Kazuhiko Kurata{2}	{1}AIST, Japan; {2}PETRA, Japan
10-Oct-19	Plenary Talk IV	09:00-09:40	09:00-09:40		Plenary	TBA	TBA	TBA
10-Oct-19	Plenary Talk V	09:40-10:20	09:40-10:20	4074	Plenary	Heterogeneous and 3D Integration at DARPA	Timothy M. Hancock	Defense Advanced Research Projects Agency, United States
10-Oct-19	Session 6: 3D Design	10:35-12:05	10:35-11:05	4086	Invited	Future Directions for 3DIC Technology and Design	Paul D. Franzon	North Carolina State University, United States
10-Oct-19	Session 6: 3D Design	10:35-12:05	11:05-11:25	4039	Lecture	Design enablement of fine pitch face-to-face 3D system integration using die-by-die place & route	Giuliano Sisto{1}, Peter Debacker{2}, Rongmei Chen{2}, Geert Van der Plas{2}, Richard Chou{1}, Eric Beyne{2}, Dragomir Milojevic{2}	{1}Cadence Design Systems, United States; {2}Imec, Belgium
10-Oct-19	Session 6: 3D Design	10:35-12:05	11:25-11:45	4037	Lecture	An Accurate Assessment of Chip-Package Interaction Is a Key Factor for Designing Resilient 3D IC Systems	Valeriy Sukharev, Armen Kteyan, Jun-Ho Choy	Mentor, a Siemens Business, Armenia; Mentor, a Siemens Business, United States
10-Oct-19	Session 6: 3D Design	10:35-12:05	11:45-12:05	4063	Lecture	Merging PDKs to build a design environment for 3D circuits: methodology, challenges and limitations	Olivier Billoint, Karim Azizi-Mourier, Gerald Cibrario, Didier Lattard, Mehdi Mouhdach, Sﾃｩbastien Thuries, Pascal Vivet	CEA, LETI, France
10-Oct-19	Session 7: Direct/Hybrid Bonding	13:30-15:00	13:30-14:00	4084	Invited	TBA	Tadatomo Suga	Meisei University, Japan
10-Oct-19	Session 7: Direct/Hybrid Bonding	13:30-15:00	14:00-14:20	4050	Lecture	A 6.9 µm Pixel-Pitch 3D Stacked Global Shutter CMOS Image Sensor with 3M Cu-Cu connections	Tsukasa Miura, Masaki Sakakibara, Hirotsugu Takahashi, Tadayuki Taura, Keiji Tatani, Yusuke Oike, Takayuki Ezaki	Sony Semiconductor Solutions, Japan
10-Oct-19	Session 7: Direct/Hybrid Bonding	13:30-15:00	14:20-14:40	4019	Lecture	Die-to-Wafer Direct Hybrid Bonding Demonstration with High Alignment Accuracy and Electrical Yields	Amandine Jouve{1}, Loic Sanchez{1}, Clement Castan{1}, Nicolas Bresson{1}, Frank Fournel{1}, Severine Cheramy{1}, Nicolas Raynaud{2}, Pascal Metzger{2}	{1}CEA, LETI, France; {2}SET, France
10-Oct-19	Session 7: Direct/Hybrid Bonding	13:30-15:00	14:40-15:00	4020	Lecture	Toward a Complete Direct Hybrid Bonding D2W Integration flow: Known-good-Dies and Die planarization Modules Development	Emilie Bourjot, Paul Stewart, Christophe Dubarry, Emmanuelle Lagoutte, Emmanuel Rolland, Nicolas Bresson, Amandine Jouve, Daniel Scevola, Viorel Balan	CEA-Leti, France
10-Oct-19	Session 8: Thermal Management	15:15-16:25	15:15-15:45	4082	Invited	Heat Transfer in Nanostructured Si and Heat Flux Control Technique	Masahiro Nomura	University of Tokyo, Japan
10-Oct-19	Session 8: Thermal Management	15:15-16:25	15:45-16:05	4033	Lecture	Vertical Stack Thermal Characterization of Heterogeneous Integration and Packages	Robert Harris{1}, Rhett Davis{2}, Steve Lipa{2}, Paul Franzon{2}	{1}GTRI, United States; {2}NCSU, United States
10-Oct-19	Session 8: Thermal Management	15:15-16:25	16:05-16:25	4042	Lecture	Thermal Stress Comparison of Annular-Trench-Isolated (ATI) TSV with Cu and Solder Core	Wei Feng, Naoya Watanabe, Haruo Shimamoto, Masahiro Aoyagi, Katsuya Kikuchi	National Institute of Advanced Industrial Science and Technology, Japan

Poster Session is scheduled on October 9 and 10. Poster session core time is 13:30-15:00, October 9.