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Fraunhofer's Initial and Ongoing Contributions in 3D IC Integration

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<Abstract>
Fraunhofer has been working on 3D integration since end of 1980´s, when they successfully fabricated 3D CMOS devices based on recrystallization of Poly-Si. Then, in a cooperative project with Siemens we were the first to demonstrate a complete industrial 3DIC stacking process (1993-1996) based on wafer bonding and vertical integration of IC devices using inter-chip vias (later called TSV). Starting 1999, we investigated 3D TSV technologies with particular focus on die-to-substrate stacking and initiated the European Integrating Projects e-CUBES®, and e-BRAINS, where we evaluated the application of 3D heterogeneous integration, including demonstration of high-performance communications. In this paper we will also present ongoing developments in heterogeneous integration and approaches for systematic hierarchical modelling in order to carry out simulations in different physical domains, based on a unified description of the 3D system.

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Peter Ramm is Head of Strategic Projects at Fraunhofer EMFT in Munich, Germany. He received Physics and Dr. rer. nat. degrees from the University of Regensburg and subsequently worked for Siemens in their DRAM facility in Regensburg, where he was responsible for the overall process integration with focus on backend-of-line. In 1988 he joined Fraunhofer IFT (now EMFT), working mainly on integration technologies for innovative devices and heterogeneous systems including the development of 3D TSV processes. Peter Ramm is co-author of over 100 publications and 36 issued patents (Europe, Japan, USA). He is IEEE Senior Member, IMAPS Fellow and Life Member, and received the Technical Achievement Award "For Pioneering Work on 3D IC Stacking and Integration" from IMAPS. Peter Ramm is co-editor of Wiley´s "Handbook of Wafer Bonding" and the series "Handbook of 3D Integration".