Fraunhofer has been working on 3D integration since end of 1980’s, when they successfully fabricated 3D CMOS devices based on recrystallization of Poly-Si. Then, in a cooperative project with Siemens we were the first to demonstrate a complete industrial 3DIC stacking process (1993-1996) based on wafer bonding and vertical integration of IC devices using inter-chip vias (later called TSV). Starting 1999, we investigated 3D TSV technologies with particular focus on die-to-substrate stacking and initiated the European Integrating Projects e-CUBES®, and e-BRAINS, where we evaluated the application of 3D heterogeneous integration, including demonstration of high-performance communications. In this paper we will also present ongoing developments in heterogeneous integration and approaches for systematic hierarchical modelling in order to carry out simulations in different physical domains, based on a unified description of the 3D system.

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