Day 1 – Thursday October 1, 2026

8:00 **Registration**

8:30 **Opening Remarks**

8:45 **Keynote Address: Sandeep Kumar Goel** *TSMC, USA*:
Standardizing the 3D Frontier: How IEEE Std P3537/3Dblox Streamlines 2.5D/3D Advanced Packaging

9:30 **Session 1: 3D Design Flow and CAD tools**

3DIC Physical Verification from a Runset Developer Perspective
Theodore Stenmark; Jean Hannouche; German Monroy; Jareer Abdel-qader; Praveen Yalavarthi; Iwonia Wirkus (Intel)

System-Level Layout versus Schematic Verification of Heterogeneous 3DIC Designs Using a Standardized 3Dblox Flow
Venkata Sai Praveen Yalavarthi; Karl Wimmer; Sreeram Gurram (Intel)

Standard-Cell Logic Folding with Heterogeneous Drive-Strength Stacking and Intra-Cell Multi-Tier Routing
Chung-Kuan Cheng; Bill Lin; Susmita Sur-Kolay; Yucheng Wang; Ying Yuan (UCSD

Placement-Evolution-Guided Cluster-Atomic Tier Assignment for Analytical 3D IC Placement
Chung-Kuan Cheng; Yucheng Wang; Ying Yuan (UCSD)

10:30 **Coffee break**

11:00 **Invited Talk: Masayoshi Tagami** *Kioxia, JP*:
CMOS Directly Bonded to Array (CBA) Technology for Future 3D Flash Memory

11:30 **Session 2: Hybrid Bonding Integration Technology**

Charge Generation and Dissipation during Wet-Chemical Surface Preparation in a Hybrid Bonding Process Module
Sungwoo Park (Samsung); Juyeol Lee (Hanyang University (ERICA); SoonAik Chew, Marko Simicic, Sven Dewilde, Nancy Heylen, Soheila Bagherilimaei, Zsolt Tőkei, Stefan De Gendt, Harold Philipsen (IMEC)

3D Interconnects for mmWave: Hybrid Bonding versus Copper Pillar up to 220 GHz
Mohammad Alsukour, Olivier Valorge (CEA LETI); Emmanuel Pistono, Jean-Daniel Arnould (Université Grenoble Alpes); Christophe Dubarry (CEA LETI)

Ultra-Thin SiCN Fusion Bonding Platform for Heterogeneous Photonics Applications
Moeen Piracha, Tom Van Der Jeught, Dmitry Kazakov, Francois Chancerel, Bryn Howells (IMEC)

12:30 **Lunch break**

13:00 **Lunch Keynote Address: Sung Kyu Lim** *U. of Southern California, USA*:
Logic Folding and Fine-Grained Logic-on-Logic 3D ICs: A Key Enabler of Tau Law

14:00 **Special Session 3 – Invited Talks: 3D Test and DfT**

14:00 **Invited Talk: Baris Arslan** *IMEC, BE*:
Exploring Test Flows and Test Access Architectures for Chiplet-Based Systems

14:30 **Invited Talk: Jennifer Dworak** *Southern Methodist University, USA:*
Hybrid Bond Die-to-Die Interconnects: An Analysis of Defects, Cluster Effects and Repair Strategy

15:00 **Coffee break**

15:30 **Session 4: 3D Architecture and Design for AI**

A scalable, high-throughput matrix transpose engine for 3D-stacked memory systems
Sushil Panda, Paul Franzon (NCSU)

TANZANITE : A 3 Layer Smart Event Sensor with Integrated AI Accelerator
P. Vivet, M. Assous, C. Socquet, S. Nicolas, S. Borel, S. Moreau, E. Ollier (CEA-LETI); T. Mesquida, M. Dampfhoffer, R. Lemaire, L. Alacoque, T. Dalgaty, S. Thuriès (CEA-LIST); S. Lacan, T. Lachaud, A. Farcy, C. Devey, P. Pierunek (STMicroelectronics); R. Poirier (Siemens-EDA); D. Joubert, G. Schon, V. Schwambach, D. Matolin, C. Posch (PROPHESEE)

System-level Simulation and Experimental Characterization of a 3D Spiking Neural Network (3D-SNN) Architecture for Hardware Reservoir Computing
Ryotaro Kawashima, Aoi Kataura, Yuqi Duan, Akihiro Suzuki, Kotaro Torazawa, Thianmontri Pattaramon, Kyojiro Kaneko, Yukino Sakurai, Takafumi Fukushima (Tohoku University); Koji Kiyoyama (Nagasaki Institute of Applied Science); Tetsu Tanaka (Tohoku University)

ROPE-MLA: Row-Access Optimized Processing Element Machine Learning Accelerator
Prasanth Prabu Ravichandiran (North Carolina State University and Nvidia); Paul Franzon, William Davis, Franc Brglez, Tianfu Wu (North Carolina State University)

16:30 **Session 5: Advanced 3D Interfaces and Memory**

Beyond Host-Side Control: HBM Controller Partitioning Across Host and HBM Base Dies
Tharunya Yogananda, Wantong Li (University of California, Riverside)

Fast Substrate Modeling for Signal Integrity Design Space Exploration of High-Speed Die-to-Die Interfaces
Eugene Chu, Shimeng Yu (Georgia Institute of Technology)

MACRO: Mixed-Signal Automated I/O Circuit Parameter Optimization for 3-D Heterogeneous Systems
Frederick Laudati, Colby Baldwin, Saibal Mukhopadhyay (Georgia Institute of Technology)

17:30 **Closing, day 1**

18:00 -21:00 **HAPPY HOUR – Food & Drinks** sponsored by Code Metal at Ormsby's: 1170 Howell Mill Rd Ste P20, Atlanta, GA 30318

Day 2 – Friday October 2, 2026

8:00 **Registration**

8:45 **Keynote Address: Rozalia Beica** *Rapidus, USA*
Heterogeneous Integration and Chiplet Architectures as the Next Scaling Paradigm

9:30 **Session 6: Advanced Interconnects**

A 15 µm Pitch Microbump Interface for 3D Die Stacking of Logic-on-SRAM
Dany-Sebastien Ly-Gagnon, Max Wu, Hans-Gerd Jetten, Aaron Liou, CH Yang, Chung-Ching Peng (Intel Corporation); Zeke Chen, Minssu Hsu, Charles Hsu (ASE Group)

Electrical Characterization and Thermal Evaluation of AlN-Infilled Fine-Pitch Cu Pillar Interconnects
Lixue Cheng, Hansol Lee, Boya Li, Dohyun Go, Andrew Kummel (University of California, San Diego); Muhannad Bakir (Georgia Institute of Technology)

Influence of Hot-Isostatic-Pressure Annealing on High-Aspect-Ratio Cu Through-Glass Vias
Murugesan Mariappan (Tohoku University)

The Energy Cost of Fewer Metal Layers in Large-Area Glass Interposers with a Core-Embedded Buffer Die
Taesoo Kim, Muhannad S. Bakir (Georgia Institute of Technology)

10:30 **Coffee break**

11:00 **Invited Talk: Robert Patti** *NHanced Semiconductors, USA*
3D Photonic Integration: Enabling Multi-Terabit Operation

11:30 **PanelDiscussion:** The Self-Sustaining Economics of a Truly Open Chiplet Market

12:30 **Lunch break**

13:00 **Lunch Keynote Address: Muhannad S Bakir** *Georgia Tech, USA*
3D Heterogeneous Integration (3DHI): Emerging Trends and Opportunities

14:00 **Invited Talk: Imene Jadli** *IMEC, BE*
From 3D Integration to Optical Interconnect: Building the Interconnect Foundation for the AI Era

14:30 **Invited Talk: Andras Vass-Varnai** *Siemens-EDA, USA*
From Silicon to System: Enabling Scalable 3D IC Packaging Through Multiphysics Simulation

15:00 **Coffee break**

15:30 **Session 7: Thermal Dissipation and Exploration**

Thermal-Aware BEOL Integration for Scalable GPU-HBM 3D Systems
Takeshi Takagi, Takeki Ninomiya,; Tadashi Kuroda (The Univ. of Tokyo)

Refresh-Aware Fixed-Point Verification for Thermal Multistability in High-Bandwidth Memory
Un Ko, Juho Kim (Sogang University)

Hybrid Flip-Chip/Wire-Bond 3D SiC Packaging Architecture for High-Temperature Applications
Jiaqi Shi, Feng Li (University of Idaho)

16:30 **Session 8: 3D Integration for Security**

3D Guard-Layer: An Integrated Agentic AI Safety System for Edge Artificial Intelligence
Eren Kurshan (Princeton University); Paul Franzon (NCSU)

Enhancing Edge AI System Security: Stacked Hardware Security Controller for Robust and Energy-Efficient Anomaly Detection
Carl Benda (NCSU); Eren Kurshan (Princeton University); Paul Franzon (NCSU)

Side Channel Attack Prevention for Post Quantum Cryptography Algorithms: A 3D-IC Based Hardware Shielding Approach
Carl Benda (NCSU); Eren Kurshan (Princeton University); Aydin Aysu, Paul Franzon (NCSU)

17:30 **Closing Remarks**