Invited Talk

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3D Integration Technologies for Stacked CMOS Image Sensors

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<Abstract>
Nowadays, the Internet-Of-Things (IoT) consists of a variety of LSIs. To use in different situations, small, multi-functional and high-performance LSIs have been strongly needed. One promising solution is System-In-Package (SiP) such as multi chip 2D package and 3D stack package. 3D chip stacking technology in particular can easily implement different function chips in a small system. We have contributed to the development of multifunctional, high-performance products with various 3D chip stacking technologies for many years. We have developed a CIS device with metal wiring under the photo-diode, which is called a back-illuminated CIS (BI-CIS). We confirmed that the device offers higher sensitivity and better performance in optical shading without any degradation in the device performance. This BI-CIS is ideally suited to applications requiring high picture quality from a small pixel size. The wafer-to-wafer bonding technology was newly introduced for the fabrication of BI-CIS. The size of CIS chips, especially for the mobile devices, were so small that the high manufacturing yield could be achieved with wafer-to-wafer bonding method. In addition to the imaging quality that conventional image sensors require, there was high demand for new functions that can respond to various photo-taking scenes. We have developed a stacked BI-CIS, composed of conventional BI-CIS technology and standard logic technology. The stacked BI-CIS layers back-illuminated structure pixels onto chips containing the circuit section for signal processing in place of carrier wafer in conventional BI-CIS. The newly attached logic circuits have achieved the advanced features such as higher sensitivity and high dynamic range (HDR) movie. In the early types of stacked BI-CIS the through-silicon-via (TSV) technology was used to electrically connect CIS chip and logic circuits. To improve the manufacturing productivity, we have recently introduced the wafer-level Cu-Cu hybrid bonding technology in place of TSV technology. The Cu-Cu hybrid bonding technology provides us further merits such as fine-pitch and large-scale connection and hence additional new functions."

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Yoshihisa Kagawa is a senior manager of Research Division, Sony Semiconductor Solutions Corporation. He received his B.S. and M.S. degrees from Kyoto University, Japan in 1999 and 2001, respectively. He joined Sony Corporation in 2004, where he has been a specialist for BEOL process integration. Currently, he manages the process integration for the CMOS image sensor. He is especially focused on developing the Cu-Cu hybrid bonding technology for staked CMOS image sensor.