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## Invited Talk

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# Future Challenges to Packaging Technologies of High Bandwidth Memory

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**<Abstract>**
High bandwidth memory (HBM) is a new and an innovative solution satisfying with semiconductor industry trends representing as the era of big data and cloud computing. SK hynix HBM1, world 1st DRAM product released in 2013 opened up the new era in memory industry by showing the excellent performance in a view of lower power and higher bandwidth and the possibility to expand the memory capacity by multi-die stacking with through silicon vias (TSVs). Starting from the high speed graphic applications, HBM is now expanding its possible applications to high performance computing, network server, accelerators and other SoC and it promotes a lot of packaging technology challenges to meet the needs of semiconductor industry market. Above all, capacity increase is one of the most important requirements for HBM. The increase not only in chip capacity but die stack count is strongly needed. However, increasing the number of stacked die is more preferable and realistic than chip capacity increase due to the limitation of transistor scaling and its poor effectiveness in chip size decrease. To adjust same die thickness with neighboring SoC die, HBM package thickness should be kept and its die thickness should be lower to achieve higher stack. Thin wafer and die handling technologies below 40um are complicated challenge in future HBM. Temporary wafer supporting system, damage-less thin die handling, and more precise die warpage control are needed. The increase in bandwidth accomplishes the increase in thermal designed power. Adding to higher stacked structure, thermal dissipation ability may get worse and it causes poor long-term transistor reliability by junction temperature increase. Power and thermal management would be a key factor to realize HBM3 or post HBM3. At the same time, a variety of package design rules should be shrunk. Finer TSV and micro-bump pitch and much narrower die-to-die gap have been continuously challenged conflicting many technical constraints. Consistent needs for both more capacity and higher bandwidth also drive another solution in system-in-package. The size limitation of a silicon interposer makes it difficult to adopt more HBM packages or larger SoC die. Si interposer can be replaced to organic interposer or RDL (redistribution layer) interposer. Direct attach of HBM to an organic substrate such as EMIB (embedded multi-die bridge) can be a good alternative to solve the size and cost problem of traditional silicon interposer technologies.

**<CV>**
Ho-Young Son received Ph.D in materials science and engineering at KAIST and has worked at SK Hynix since 2008. Now he is a principal engineer and in charge of wafer level package development such as 3D TSV, flip chip bump, fan out wafer level packages, and its process integration. Developed world first 8hi memory stack (2Gb*8hi) using TSV in 2011. Led HBM (high bandwidth memory) Gen1 development as the world first HBM product in 2013 and HBM2 in 2016 and 3DS DDR4 based 128GB LRDIMM (Load Reduced DIMM) in 2014 and implemented mass reflow processes for multi-die stacking in 2016. Now leading all of wafer level process development in SK Hynix including HBM2E and HBM3, which is upper version of HBM2, DDR5 3DS, cost effective RDL (redistribution) and CPB (copper pillar bump)/micro-bump technologies. Also he is looking for advanced technologies like homo- and heterogeneous stack solution of DRAM multi-die or DRAM/logic dies.