Invited Talk

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Power-Performance Advantages of InFO Technology for Advanced System Integration

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<Abstract>
Since 2012, the development of InFO technology has gained much attention in semiconductor industry as it leads a new wafer level system integration (WLSI) development direction. The technology leverages foundry wafer process experience and Cu back end of line (BEOL) capability to provide thin dielectric layer, fine pitch RDL and vertical interconnect for system designers the flexibility to design 3D system, multiple chip system and RF/Analog system, respectively. The InFO has a unique position in the TSMC WLS I platform from package size and IO counts for mobile, IoT and HPC applications. In the paper, the power integrity, signal integrity and RF performance of the technology in the applications will be reported. For power integrity, excellent performance from thin dielectric layers and integration of low equivalent series inductance (ESL) integrated passive devices (IPD) is studied. The technology has 38% lower power delivery networking (PDN) impedance and 17% lower voltage droop, compared to flip chip substrate. For bandwidth performance, the effect of line width on data rate and line density is studied. At the finest line width, the InFO can provide more than 1,000/mm interconnect lines between chips. The bandwidth density for the finest line (1x) is about 2.5 times higher than that for the coarse line (2.5 x). The bandwidth densities of various technologies, such as MCM, Fan Out, Si Bridge, Si Wafer and InFO are compared. A record high 10 Tbps/mm of bandwidth density is obtained by submicron RDL In FO. Finally, a 3D solenoid InFO inductor is demonstrated. The inductor, formed by Cu via and RDL achieve s 0.68x lower resistance and 1.6x higher Q factor, compared to 2D spiral inductor at the same inductance. From the above study, we can conclude the InFO technology provide s superior power performance advantages from thin dielectric and flexible RDL pitch for mobile to HPC product applications.

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Chuei- Tang Wang received the B.S. and M.S. degrees in materials science and engineering from National Tsing Hua University, Hsinchu, Taiwan, in 1983 and 1985, respectively, and the Ph.D. degree from Stanford University, Stanford, CA, USA, in 1997. He joined USI in Nantou, Taiwan and led wireless connectivity SiP module design in 1999. Later he was responsible for system miniaturization technology development. In 2011, he joined TSMC Integrated Interconnect and Packaging (IIP) RD team as a Technical Director for system architecture and SI, PI and RF performance study. He had received a National Award of Industrial Technology Advancement (ITA), Taiwan, for the leadership of connectivity SiP module development in industry in 2007. He holds 60 US patents.